DESIGN NOTES

This board is designed to have up to four AB0003 OEM A2B modules plugged in to provide a compact way to have multiple A2B nodes for general software development and system prototyping. All nodes are set to run as locally powered A2B slave nodes. (see Clockworks website for master nodes and other configurations).

This is very much a utility board and not meant to be an elegant piece of engineering.

LEDs
The GPIO can sourcne or sink reasonably symmetrically, and it's easier to have a "1" turn the light on when testing. It also means we don't need to try and match the VIODD jumpering on the module in terms of applying 3.3 to a 1.8V pin (which is a no-no on this part).

The AD2428's I/O supply will power the LEDs, and it's nominally limited to 20 mA typical (datasheet #). With 10 LEDs that means 2 mA per LED. Fine, nobody like to be blinded by LEDs.

To help identify them half are red and half are green.

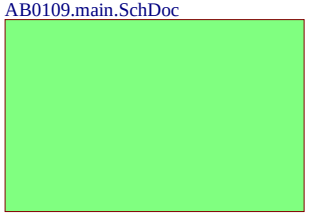
For the LiteonLTST-C150 series LEDs used Vf for the green is about 1.85V and red is 1.65V at the 2 mA point. That works out to Rs of 725 ohms and 825 ohms, respectively, with V = 3.3. Actual output voltage is about 3.2V in the high state. Closest E24 values are 750 and 820 ohms. Measured Vf for the green LED is about 1.9V @ 1.5 mA. That does mean if VIO is jumpered for 1.8V the green LEDs are probably not going to light up.

Note:
CircuitStudio back annotation is a bit odd with hierarchy, so while it was done the results might not quite be what you might expect.

REVISION HISTORY

Rev 1: Created.

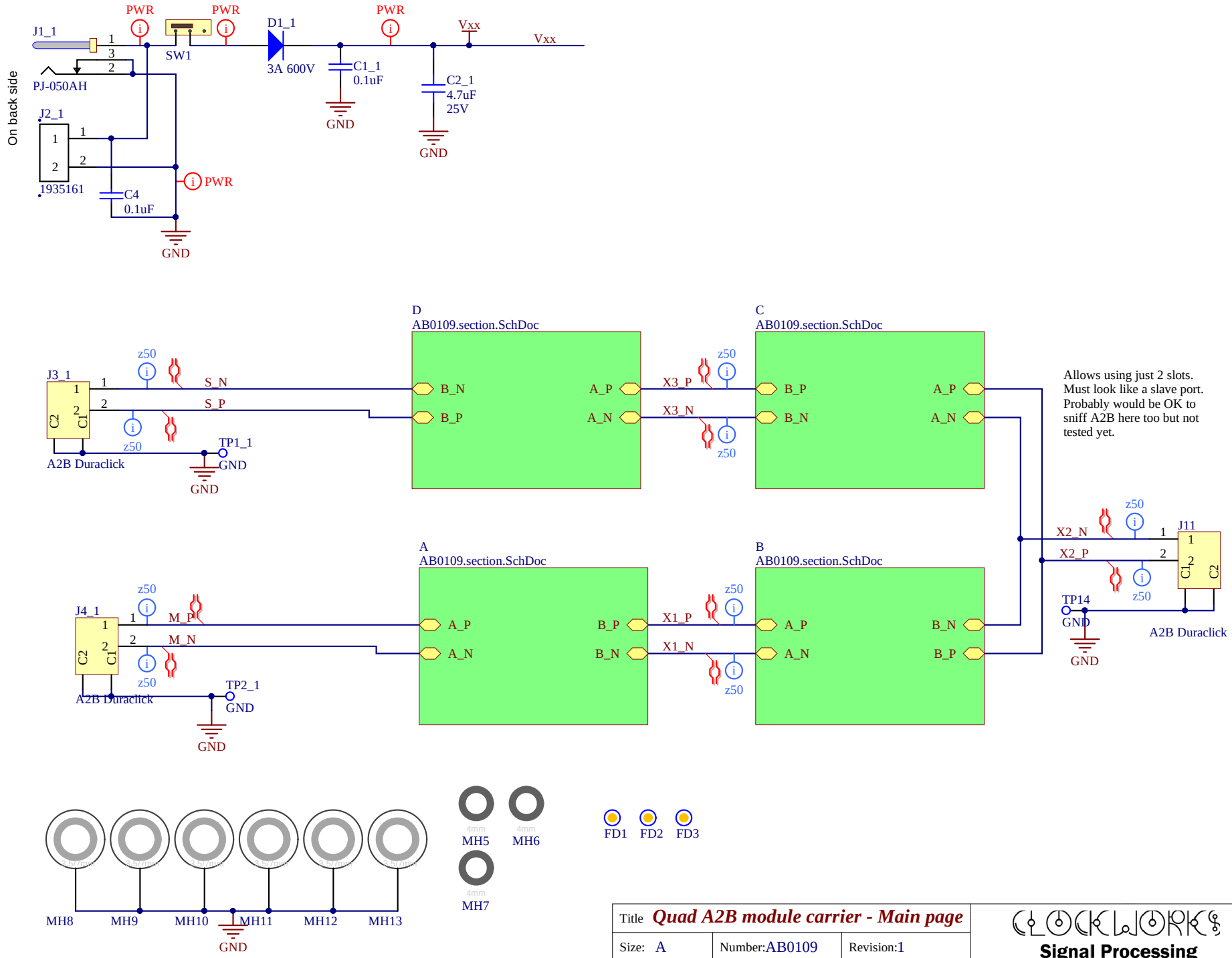
Top page
AB0109.main.SchDoc



© 2020 Clockworks
Signal Processing LLC

Title	*Quad A2B module carrier - Cover page*		
Size: A	Number: AB0109	Revision: 1	
Date: 6/24/2020	Time: 9:12:04 PM	Sheet 1 of 3	
File: AB0109.cover.SchDoc			

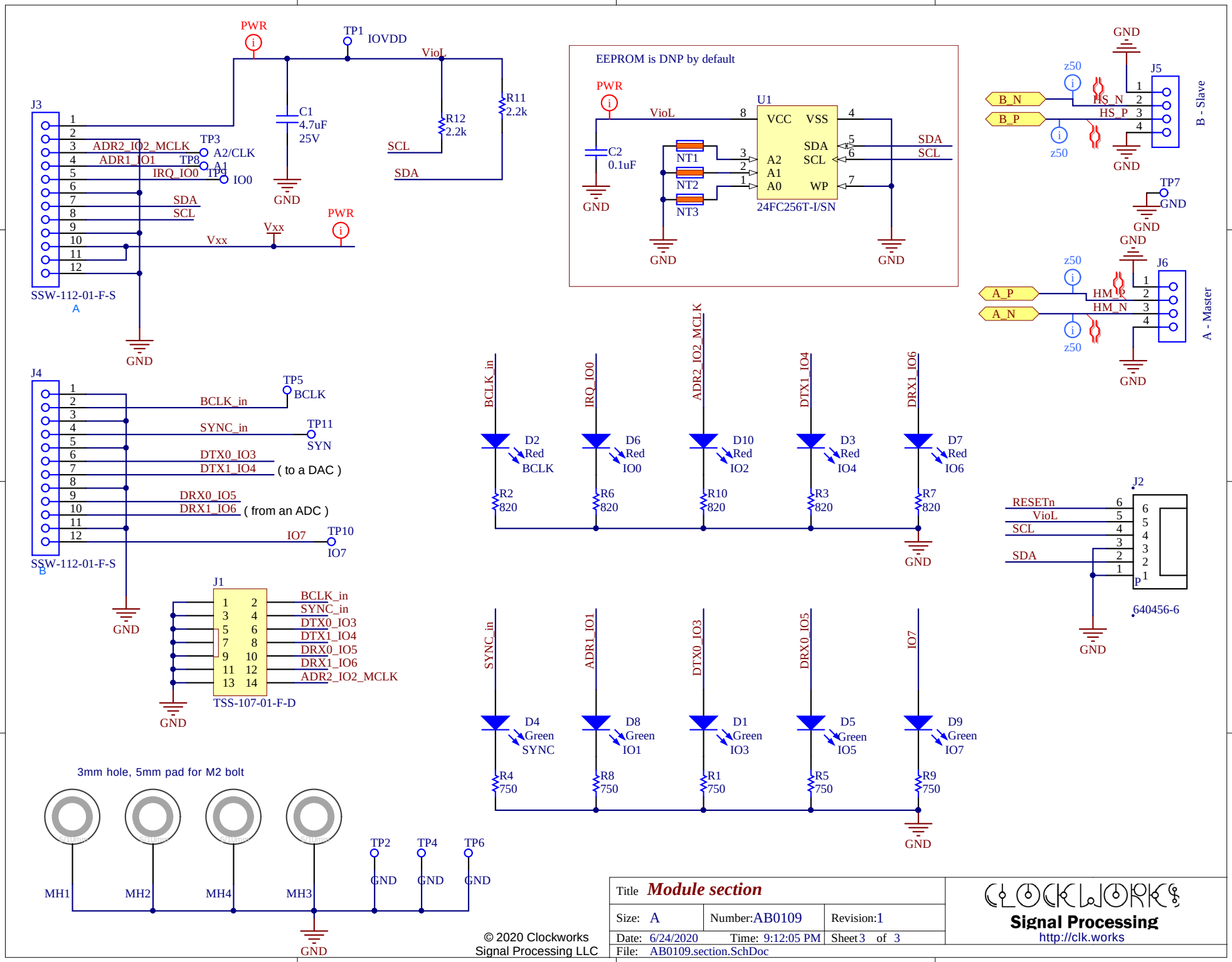
CLOCKWORKS
Signal Processing
http://clk.works



Title	*Quad A2B module carrier - Main page*	
Size: A	Number: AB0109	Revision: 1
Date: 6/24/2020	Time: 9:12:04 PM	Sheet 2 of 3
File: AB0109.main.SchDoc		

CLOCKWORKS
Signal Processing
http://clk.works

© 2020 Clockworks
Signal Processing LLC


PWR
TP1
IOVDD
VioL
J3
SSW-112-01-F-S
A
ADR2_IO2_MCLK
ADR1_IO1
IRQ_IO0
TP3
A2/CLK
TP8
A1
TP9
IO0
SDA
SCL
Vxx
C1
4.7uF
25V
R11
2.2k
R12
2.2k
GND
EEPROM is DNP by default
U1
VCC
VSS
SDA
SCL
A2
A1
A0
WP
24FC256T-I/SN
C2
0.1uF
NT1
NT2
NT3
J5
B - Slave
B_N
B_P
HS_N
HS_P
z50
TP7
J6
A - Master
A_P
A_N
HM_P
HM_N
J4
SSW-112-01-F-S
B
TP5
BCLK
BCLK_in
TP11
SYN
SYNC_in
DTX0_IO3
DTX1_IO4
(to a DAC)
DRX0_IO5
DRX1_IO6
(from an ADC)
IO7
TP10
J1
TSS-107-01-F-D
D2
Red
BCLK
D6
Red
IO0
D10
Red
IO2
D3
Red
IO4
D7
Red
IO6
R2
820
R6
820
R10
820
R3
820
R7
820
D4
Green
SYNC
D8
Green
IO1
D1
Green
IO3
D5
Green
IO5
D9
Green
IO7
R4
750
R8
750
R1
750
R5
750
R9
750
J2
RESETn
VioL
SCL
SDA
640456-6
3mm hole, 5mm pad for M2 bolt
MH1
MH2
MH4
MH3
TP2
TP4
TP6
© 2020 Clockwork
Signal Processing LLC
Title Module section
Size: A
Number: AB0109
Revision: 1
Date: 6/24/2020
Time: 9:12:05 PM
Sheet 3 of 3
File: AB0109.section.SchDoc
Signal Processing
http://clk.works