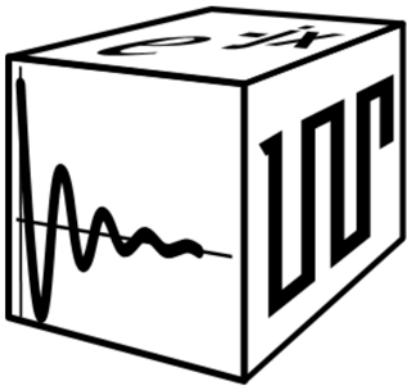
SIGNALBLOX®



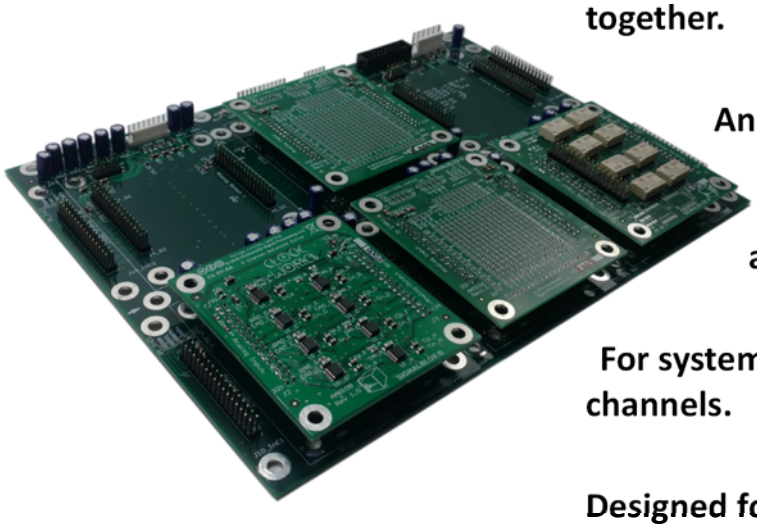
CLOCKWORKS
Signal Processing

OPEN SOURCE MODULAR HARDWARE FOR SIGNAL PROCESSING

SignalBlox®
Design Guide

Cost effective, off-the-shelf hardware built for real world signal processing applications.

Create complex systems quickly by plugging modules together.



Example populated AnalogBlox 3 deep by 2 wide carrier for analog processing of 16 balanced input channels. For clarity shown without input and output connector modules.

AnalogBlox modules for analog signal manipulation can be combined with DigitalBlox mixed signal and DSP modules across a wide range of applications

For systems with channel counts from 8 to 256+ channels.

Designed for developers, designers, and OEMs.

Open source hardware: modify and reuse.

AnalogBlox complements the DigitalBlox hardware to offer standard connectors, buffering, level control, and switching for analog input and outputs.

Control via I^2C from Arduino, Raspberry Pi, etc.

Designed to work with Analog Device's SHARC® Audio Module and A^2B® technologies.

SignalBlox, AnalogBlox, and DigitalBlox are trademarks of Clockworks Signal Processing LLC.

A^2B and SHARC are trademarks of Analog Devices Inc.

Organization of this guide

This document offers guidance to develop an understanding of the system creation process. If you need further details of the hardware all SignalBlox module and carrier schematics are available. In this document you will find information on the signals and connectors used in the AnalogBlox and DigitalBlox systems.

There are separate documents available from Clockworks website Reference section that cover mechanical aspects and also have simplified pinout lists for the connectors.

Overview

SignalBlox modules and carriers offer a huge range of possibilities for creating signal processing systems in hours. With their open-source hardware design users have the opportunity to customize functions and features while still benefitting from a large collection of off the shelf hardware.

With standardized mechanical and electrical characteristics for both modules and complete carrier systems designers can instead focus on their unique project requirements and not spend effort on run-of-the-mill aspects.

Easy software integration, with examples being developed for the SHARC Audio Module that can be ported to other development tools like Arduino and Raspberry Pi to further accelerate project development.

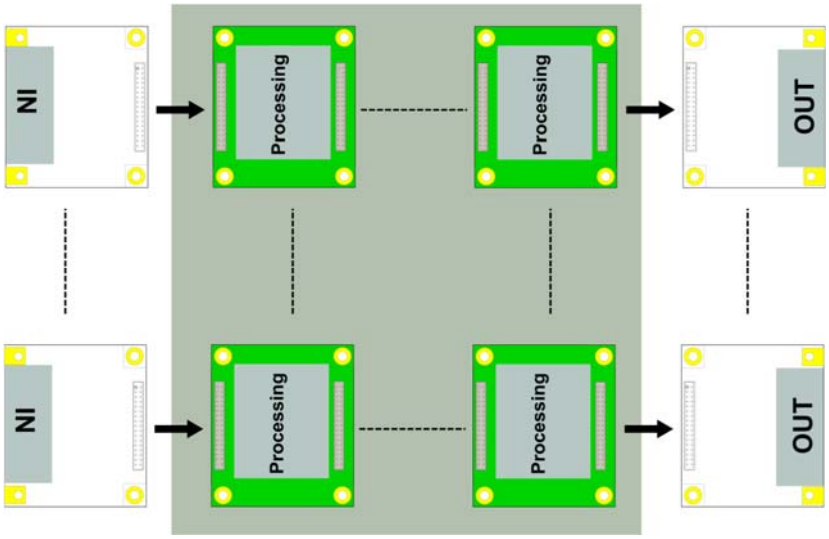
Modules can be daisy chained by plugging them in to carrier boards to construct complex systems. They can also be added in parallel to create high channel count systems. Modules are sized to allow four to be placed in parallel on a carrier card inside a standard 19" rack mount enclosure; this can provide 32 inputs and 32 output channels in a 1U height with standard eight channel modules and 64 inputs and outputs with double density sixteen channel modules.

The AnalogBlox product line has features not normally associated with prototyping hardware: ESD and RFI protection on inputs and outputs, MUTE relays on the outputs for click & pop free audio, control over analog power sequencing, and standard multiple supply voltages to accommodate a range of applications without needing complex and costly on-module power supplies.

AnalogBlox systems will typically be used as the front or back end to DigitalBlox systems. While described in terms of audio applications, most AnalogBlox modules can be used for any type of analog signal that fits the bandwidth and voltage levels of the module.

DigitalBlox provide both mixed signal Analog to Digital (ADC) and Digital to Analog (DAC) conversion along with either digital data interfaces (I2S), Analog Device's A^2B (up to 32 channels on twisted pair) or DSP via Analog Device's SHARC Audio Module.

© 2020 **Clockworks Signal Processing LLC**



Open source hardware

All SignalBlox modules are considered open hardware with the design files available under the Creative Commons CC 4.0 share-alike by attribution license. You are free to copy and modify the design for any purpose, however you must publish your source (design files) as well as include attribution to Clockworks Signal Processing LLC to remain in compliance with the license granted to you by Clockworks Signals Processing LLC.

If your business can not comply with the Creative Commons SA-BY license a commercial (proprietary) license is available from Clockworks Signal Processing LLC for a nominal charge.

SignalBlox and the cube logo are trademarks of Clockworks Signal Processing LLC and you may not use those nor make any reference to SignalBlox in your product or any description of your product. You take full and complete responsibility and all liability for use of a Clockworks Signal Processing LLC provided designs as well as any modifications made by you or others.

Signal Processing

Carrier Boards

Carrier boards provide a way to configure AnalogBlox and DigitalBlox modules in to a complete system. Currently two classes of carrier designs are defined, one that is for “all analog” use and the other that is for digital and mixed signal use (i.e. ADCs, DSP, DACs) with the ability to interconnect different carrier boards to create application specific configurations.

As with other SignalBlox hardware, all of the carrier designs are available for modification to meet the needs of a specific application requirement.

In addition to the SignalBlox module connectors, the carrier boards have a standard set of connections for system power and control. The last part of this guide provides the details of the connectors; they can be summarized as:

Digital power in

- Type: 12 pin .1” MTA-100
- Power: 3.3 standby, 3.3 V, 5V
- Control: DIGPOWERn, PWRGOOD

Analog power in

- Type: 8 pin .1” MTA-100
- Power: +/- 5V, +/- 15V
- Control: ANAPOWERn

HVHC Aux power in

- Type: 6 pin .156” MTA-156
- Power: +48, +HV, -HV

Control

- Type: 20 pin .1” (2.54mm) dual row
- Power (out): 3.3 standby, 5V
- Control: I^2C + interrupt, mute (2), RESETn, power control/status (3), Timing (2)

Aux Control

- Type: 6 pin .1” MTA-100
- Power (out): 3.3 standby
- Control: I2C, RESETn

© 2020 **Clockworks Signal Processing LLC**

AnalogBlox®
Carrier Boards

Carrier boards provide a simple way to interconnect modules and provide the needed connectors for power and control. One of the key capabilities of the carrier boards is to route I^2C to allow multiple identical modules with I^2C control - and therefor conflicting I^2C addresses - to be uniquely addressed.

AnalogBlox carrier boards can carry any of the analog processing modules and connect to analog input or output modules at the edges.

Systems can be configured in any compatible module order and custom carrier systems can support differing module chain lengths.

For OEM applications it is practical to merge the module design with the carrier design to create a custom system. This typically lowers the per unit cost by about half since it's now one PCB instead of two and the bulk of the connectors are eliminated. Hybrid systems of built-in functions plus modules are also easily created.

While not the same feature set as the carrier boards, the AA0106 prototyping module can be used as a carrier by installing two headers on the top instead of the normal bottom mounted sockets. Discrete wires can then be connected to the signal line breakouts. This can be helpful for testing modules in isolation without any complications from the more sophisticated design of the carrier boards.

DigitalBlox®
Carrier Boards

The DigitalBlox carrier boards are somewhat more complicated than the AnalogBlox ones as they work with a combination of analog and digital (I^2S) signals. Since modules have specific functions, i.e. analog to digital, digital to analog, or digital to digital, they must be plugged in to specific module sites.

Analog signals are carried on 34 pin connectors and the digital ones on 40 pin connectors; to the extent that one pays attention when plugging in modules configuration is a straight forward undertaking.

Mixed signal systems do have a consideration for clocking that must be evaluated during the system design process. Normally all ADC and DACs should be operated off of the same master clock and have the same frame syncs to ensure that all channels sample synchronously.

© 2020 **Clockworks Signal Processing LLC**

CLOCKWORKS
Signal Processing

Power Supplies for SignalBlox systems

One of the first system design issues in a mixed analog and digital design is what to do about power supplies. Low end consumer audio systems can operate the analog on +5V-only; high performance application will require split-rail supplies. While most analog functions can use +/- 15V supplies, there are devices that require other analog voltages.

Once the voltages are determined the issue of supply current comes in to consideration. The cost of a supply is somewhat of a step function, for example if you need 1 amp the cost might be X, but the next size up might by 2 amps at a cost of 1.5X so if you need 1.2 amps you're paying for the next size.

It is not possible to optimize multivoltage supplies for general use and lowest cost configurations, a custom supply design would need to be created. While this makes sense for systems sold by the tens of thousands it isn't practical for the majority of applications.

During development bench supplies can be used but with a large number of voltages needed they are somewhat impractical as well as not supporting the standby/sequencing that most real world systems will need.

Clockworks currently offers two different supplies. Both use an external 12 VDC supply as their primary input as that also solves the problem of connecting to the AC mains on a worldwide basis with units that meet each region's safety and EMC requirements.

© 2020 **Clockworks Signal Processing LLC**

© 2020 **Clockworks Signal Processing LLC**

3D rendering of a typical input module, shown with typical mounting brackets

Signal Processing

AnalogBlox®

Signal and design summary

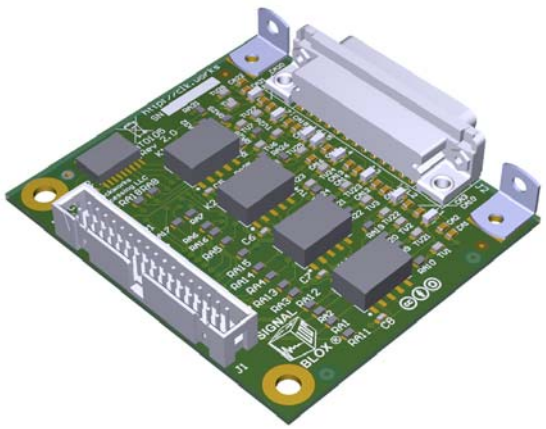
Overview

AnalogBlox modules are generally all the same physical size, 75mm x 85mm (2.95” x 3.35”). An exception in that size for input and output modules may exist for boards with certain large input or output connectors like XLRs.

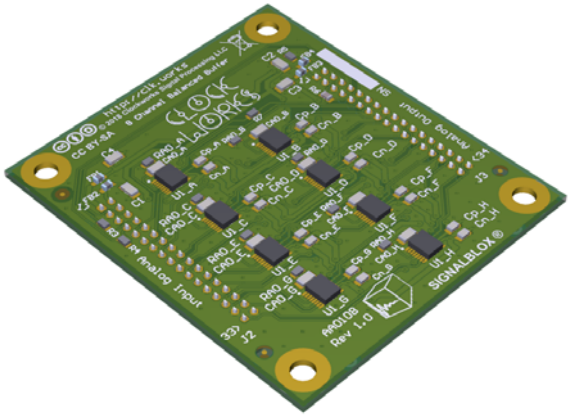
Analog input modules have an input connector (RCA, DB25, etc.) designed for flush mounting against a rear panel, with pads and a pair of holes for a Keystone #613 bracket. A 34 pin shrouded header is installed on the top side for mating with a ribbon cable, as illustrated in the figure on the top of this page.

Analog output modules mirror the input module, as illustrated by the second drawing.

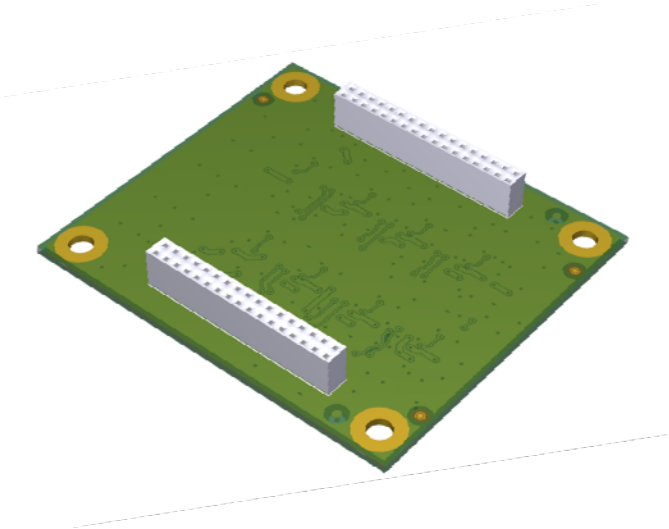
Analog processing modules, i.e. modules with an in and out connector, are normally provided with two 34 pin sockets on the bottom side of the board. The exception is the prototyping module AA0106, which is assembled by the user with the desired socket/header configuration on either the top or bottom.



3D rendering of a typical output module, shown with typical mounting brackets



3D rendering of a typical analog processing module, top view.



3D rendering of a typical analog processing module, bottom view.

© 2020 **Clockworks Signal Processing LLC**

+15	1	2	-15
GND	3	4	+3.3
GND	5	6	RESETn
SDA	7	8	SCL
MUTEn / INTn	9	10	GND
1 (+)	11	12	1 (-)
GND	13	14	2 (+)
2 (-)	15	16	GND
3 (+)	17	18	3 (-)
GND	19	20	4 (+)
4 (-)	21	22	GND
5 (+)	23	24	5 (-)
GND	25	26	6 (+)
6 (-)	27	28	GND
7 (+)	29	30	7 (-)
GND	31	32	8 (+)
8 (-)	33	34	GND

Analog (primary) connector pinout

1	-5 VA
2	GND
3	+5 VA
4	GND
5	+5VD
6	GND
7	+48 VA
8	+VAPWR
9	GND
10	-VAPWR

Aux (secondary) power connector

Modules have 4mm holes located in the corners (except for the input and output modules with mounting brackets). An M3 bolt can be used with a conductive standoffs. Standard 2.54 mm (0.1”) socket and header strips have a 11mm (approx. 7/16”) mated height.

Analog Connectors

This section looks at the connector signals in detail and how they are normally implemented in an AnalogBlox system. Processing boards have two of these connectors. Pin 9 (MUTEn/INTn) has a different use between input and output sides.

While there is a convention for these signals defined at the module level, the use of these signals at a system level is defined by the carrier card that the modules are used with.

Through hole connectors with the same dimensions as the Samtec TSW (header) and SSW (socket) series parts should be used to ensure consistent mating heights and reliable operation.

Power

The power budget for each module is a function of the system size and the power supply used with it. For the primary connectors (total per module) +/- 15V supplies (pins 1 and 2) 300 mA per board is budgeted. For pin 4 of the connector, 3.3V at 1 A is budgeted.

For the secondary power connector the +/- 5V analog supply is budgeted at 200 mA for the module and the 5V digital at 1A per module. No budget is defined for the +48 and +/- VAPWR as those are a function of the system design. A design maximum of 3A per connector pin should be observed.

Control

Modules are controlled over standard I^2C bus. It should be operated at 100 kHz unless all modules are available to operate at 400 kHz. Pullups are not present on modules.

By default modules connect the I^2C pins on the input and output connectors through two installed 0 ohm jumpers even if they do not use I^2C. Carrier boards may follow different rules on which connector’s I^2C pins they expect to control the module through.

Modules that use I^2C may have situations where they monitor for various changes of status that may indicate (for example) a fault condition. In large systems with many modules polling for status over I^2C is time consuming and the interrupt line (pin 9 on the output connector) should be used to indicate a module should have its status read.

All modules that have devices that use an external reset input must connect that reset signal to the connector’s RESETn signal, (pin 6) which is active low. The system will assert RESETn until all digital supplies are stable. RESETn may be asserted low at other times by the

system control processor. Modules may mute their outputs on assertion of RESETn but it is not mandatory.

Modules should connect the two RESETn pins from each connector.

If a module has a way to mute the output signal this should be implemented via pin 9 of the input analog connector. By default modules should not propagate the MUTEn signal on the input connector to the INTn signal on the output connector as they have different functions. The carrier board will propagate a host processor mute request directly to all modules.

Analog module design guide

This description provides general guidance which may or may not be appropriate for your own custom design.

Drawings of the board outlines, STEP files, and other mechanical information is available.

Power

Treat the incoming DC power nicely. While nominally there is a concept of quiet analog supplies for powering things like op-amps and ADC/DACs, designs should not therefor treat the digital supplies as place to generate noise as that noise will find its way in to other parts of the system, or even worse find its way out of the system and in to other connected equipment.

High frequency noise can and will couple in to the audio band in all sorts of strange and marvelous ways. For digital parts used anywhere in the system do not rely on spread spectrum clocking to solve a noise problem—all those do is spread the noise across the audio band. While this is less objectionable than tones, the correct approach is to not radiate the noise in the first place.

The carrier boards provide bulk decoupling capacitance for the supplies as well as smaller ceramic capacitors at each connector. By virtue of the physics involved they are limited to reducing noise below a few MHz at best. Supplies should be well decoupled for high frequencies on the module.

Control signal considerations

Handling of the few control signals is a straightforward application of the discussion in the prior section, with one notable exception regarding mute. If a processing module can determine that the output needs to be muted but for some reason can not mute its own output there is no direct way to support that as the only output is the INTn signal. If the condition leading to a mute state can be detected then the host processor would need to respond to the interrupt from the INTn line, scan the I^2C devices for status, and then effect a mute state on the downstream modules. This can easily take several milliseconds.

Given how unlikely it is that an analog module will be able to determine that a muted signal state is appropriate it's reasonable to take this discussion as a highly improbably corner case. If it appears in a real system configuration it may be solved by the carrier board treating INTn on the output as MUTEn on the input of the downstream module.

There is one additional consideration regarding MUTEn use - it applies to all channel on a module. Most likely in an analog only system a mute state is only needed on specific signals. (At a DAC to analog out boundary this is probably not the case.) Generally there is no transverse application of a mute state request across other channel strips (i.e. modules handle 8 channels at a time and operate autonomously from each other).

The best method for handling these complex corner cases will need to be decided by the system designer and may require customization of the carrier board.

Analog Signals—levels

There are 8 balanced lines on the connector. There is no standard signal level as it is dependent on the input signals and/or the intended output. Consumer system generally treat 316 mV RMS (-10 dBv/-7.8 dBu) as full scale signal, except at the connection between a preamp and amplifier, where 1 to 2 V RMS (0 dBV/2.2 dBu — 6 dBv/8.2 dBu) for driving the amp in to clipping is common; there are a few amplifiers that might require > 2V RMS . The tradeoff for max output and useful SNR without costly ultra low noise components is a complex one.

Pro audio levels vary across a wide range. Theoretically +4 dBu (1.8 dBv/1.2 VRMS) is the nominal level. When used with a balanced connection the P-P voltage on each signal line is one-half the total.

Many systems with balanced outputs can drive levels of +14 dBu (3.9V RMS), +20 dBu (7.75 V RMS) or even +24 dBu (12.3 V RMS). With systems based on ICs these high voltages can be troublesome. +14 dBu is 11 V P-P or with a balanced signal 5.5V P-P on each wire. ADC inputs are typically less than 3V P-P, meaning the input buffer stage is actually an attenuator.

On the output side 20 dBu can be achieved with op-amp run on +/- 15V supplies, though as output voltages approach the rails the op-amp distortion can increase as well as possible issues from slew rate in ultrawide band audio applications.

In the AnalogBlox system the +/- analog supplies are always +/-5 and +/-15. The two undefined power pins can be used to carry the +/- 18V that is typically used for the drive stage for the high > 20 dBu levels.

As with the consumer (lack of) standards, the range of pro levels and optimizing SNR becomes a complex problem.

Analog signals—balanced vs. single ended

Modules that output only a single ended signal should ground the “-” output. Modules that only have a single ended input should use the “+” input and leave the “-” input disconnected.

For a collection of small modules on a carrier board and careful system design there isn’t any inherent advantage to balanced signals over single ended as there shouldn’t be additional noise to be picked up inside of the system enclosure. The signal length is short compared with use cases like microphone cables or long runs between equipment in EMI hostile environments.

It can be convenient though to leave the signals balanced as many ADCs and DACs operate that way.

There are a couple of considerations in module design: if the signal is converted from balanced to single ended then a design with high common mode (CM) rejection should be used as there will be no way to remove the noise later in the system. This same concern can be true of designs that are balanced input and output, they must not behave in a way where mode conversion occurs and ideally will reject CM noise.

The balanced buffer module can be used for both impedance buffering and CM rejection.

If the AA0108 THAT buffer module is used with single ended inputs and balanced output then keep in mind this represents a +6 dB signal gain since the P-P voltage is now twice as high.

© 2020 **Clockworks Signal Processing LLC**

Carrier board standard connections

In addition to the connectors on the AnalogBlox and DigitalBlox modules, carrier boards have a number of power and control connectors that may also appear on other portions of a SignalBlox system.

This section provides some additional details about these connectors. The carrier board schematics can also be informative for understanding how you may want to copy them for a custom design.

Primary Digital Power

This is a 12 pin MTA-100 series connector. The table shows the standard wire colors used in Clockworks systems, which is loosely based on PC power supply standards.

Pin	Signal	Wire color
1	+3.3STDBY	purple
2	+5	red
3	GND	black
4	GND	black
5	+5	red
6	+3.3	orange
7	+3.3	orange
8	GND	black
9	+3.3	orange
10	DIGPOWERn	green
11	PWRGOOD	grey
12	GND	black

Primary digital power connector

3.3STDBY is always on and one amp is available. For CE standby compliance the system power must be less than 500 mW, and this has to include the power supply losses. In most systems that aren't wake-on-LAN this works out to about 100 mW being available to power a small micro that can handle soft power key or IR remote requests.

+5 and +3.3 are switched on by the DIGPOWERn signal being in a low state. The largest carrier board (4 strips of modules) should limit the load on +5 to 4 amps and 10 amps on +3.3, or the supply limits, which ever is less.

DIGPOWERn is expected to be pulled high on power supplies, therefor during system power up if nothing pulls the DIGPOWERn signal low only the 3.3V standby will be powered.

Carrier board designs should assume they can place up to a 500 uF capacitive load on the +5 and +3.3 supplies. Conversely the load capacitance should be a consideration in the power section design.

PWRGOOD is an indicator of the primary power input, not that all supplies are in spec. PWRGOOD should be an interrupt input to the system control processor that can place the system in a safe state (mute outputs, etc.) within the hold up time of the supply. The Clockworks supplies have a time delay on the PWRGOOD signal to give the supplies enough time to stabilize.

A host that is controlling the digital (or analog) power enable signals must either wait or monitor those supplies to determine they are stable enough to enable the associated circuitry.

Analog power

This connector is a 8 pin MTA-100 series connector and provides the voltages typically used by op-amps (+/-15) and ADC/DAC chips (mostly +5, but –5 available). Some ADC can be damaged by high input voltages and clamping circuits can create as many problems as they solve so the +/- 5V can also helpful in some ADC input buffer circuits to avoid overdriving the ADC.

Pin	Signal	Wire color
1	ANAPOWERn	green
2	+5	pink
3	GND	black
4	-5	white
5	GND	black
6	+15	yellow
7	GND	black
8	-15	blue

Analog power connector

The ANAPOWERn should be pulled low to enable the analog supplies.

When creating a module that uses a number of voltages keep in mind that there is no specified sequencing. The analog +/-15 and +/-5 supplies could be held in the off condition for a long time.

Multivoltage parts with specific supply sequencing needs are most likely best powered by local regulation from the +5V digital supply.

The analog supplies are nominally clean/low noise and hanging switching regulators off them for local supplies may increase system noise.

HVHC Auxiliary Analog Power

This connector is the High Voltage, High Current connector. It's intended to supply analog power for some of the less typical applications. It uses a MTA-156 series connector to ensure mechanical incompatibility with the other connectors used in the system.

Pin	Signal	Wire color
1	+48	-
2	GND	black
3	+HV	-
4	GND	black
5	-HV	-
6	GND	black

HVHC Auxiliary Analog power connector

There is no explicit enable for this signal but is normally assumed to be the same ANAPOWERn signal used for analog supply enables.

48V is supplied for cases where phantom power is needed for an XLR input connection for microphone power. Custom connector modules are needed in that case as the ESD features in standard modules have a typical clamping voltage of 24V.

The +HV and –HV voltages are unspecified but should be limited to less than 48V. They are intended to provide power to things that need a voltage different than the stand voltages.

Theoretically they could also power an output amplifier section—the limiting factor will be the maximum current of the module's Aux Power connector (3 amp/pin max) and not the MTA-156 pin. Driving eight 4 ohm speakers with a power budget of 1 amp (average) is not going to go very far and the system design should include a separate power connection. 8 channels at 10 watts/channel is possible with class D amps in the module size, which is about 13 amps with 4 ohm speakers.

Power sequencing

A typical system will operate as follows when powering up:

- Standby supply is powering a small microprocessor waiting for an on event. (IR, software power button, network, trigger, etc. Systems with a hard power switch skip this). Analog output mute held low.
- Standby microprocessor turns on digital supplies and waits for the primary processor (if present) to indicate it has booted. Outputs still muted.
- Host processor places digital peripherals in safe operational states.
- Analog power enabled

- All digital and analog sections places in zero signal/max attenuate state
- Analog mute released
- Processor increases signal levels to operational state slow enough to avoid artifacts (typically a few hundred msec).

On an orderly shutdown the reverse of the above sequence is performed. Cases where there's an input loss of power, which includes a system with an AC mains wired On/Off switch, will need to perform the reverse of this sequence as soon as loss of power is detected.

The supply hold up time is most likely limited to a few milliseconds so the signal ramp down time will be much shorter and could produce some artifacts if the signal output was at full scale levels when power was removed.

Control connector

This 2x10 .1" header is intended for a small "host" processor to control the carrier board's functions. These are broken in to several categories 1) things controlled by GPIO, 2) things controlled over I2C, 3) power, and 4) the mystery signals.

Direction in the table is relative to the carrier board.

pin	signal	direction	notes
1	+5	out	regulated, 1A "Digital", Off in standby
2	+3.3STDBY	out	regulated, 1A, Active in standby
3	GND		
4	GND		
5	SDA	i/o	I2C data
6	SCL	i/o	I2C clock
7	INTn	out	I2C INT req input
8	GND		
9	MUTEOUTn	in	Output (DACs) normal mute - is OR'd with other mute sources
10	OUTOFFn	in	Hard output mute (Analog output) - is OR'd with other mute sources
11	FAULTn	out	Fault from carrier
12	GND		
13	DIGPOWERn	in (OC)	Output to place primary power in standby mode
14	ANAPOWERn	in (OC)	Output to enable analog supplies
15	RESETn	in (OC)	Reset entire carrier
16	GND		
17	PWRGOOD	out	Power input good
18	SYNC	i/o	System sync reference
19	GND		
20	TC	i/o	Time Code

Control connector—power

The carrier provides power to the processor board that can be connected to the control connector. 3.3V is available for operating the system in a lower power standby state (assuming the power supply supports this feature). The power supply should offer up to 1A for powering the processor in its normal run state, and be designed that 100 mW is available to the processor in the standby state with the system meeting the 500 mW allowed maximum. Systems with AC line power switches do not need to worry about this.

5V is also provided as many host processors will have a USB Host port. This digital +5 is part of the switched power and that should be kept in mind if the processor has particular sequencing requirements.

Control connector—I^2C

The I^2C bus is pulled up on the carrier board to keep it in a valid state for cases where a host processor isn't used. Some processors boards may also have pullups on them and while two sets of pullups are usually OK it should be confirmed as part of your system design.

Carrier boards have addressable I^2C muxes to select a module location uniquely. This allows the same module to be used multiple times as most I^2C devices lack a large address selection space.

The interrupt line is considered part of the I^2C interface. Polling I^2C is slow and inefficient and interrupts should be used to signal to the host processor that something needs attention. The I^2C mux on the carrier board provides routing of interrupts as well so limited polling is needed to determine where the interrupt came from.

I^2C address space issues with multi-carrier systems must also be considered, but that topic is more complex than the general introduction here.

Control connector—control signal

There are a number of signals that would typically be connected to GPIO lines on a control processor.

MUTEOUTn—this line should be pulled low to place any active electronics on modules that support a MUTE state in to that mode. On a carrier board the MUTE state can also be created by a module, though that's mostly a consideration for the DigitalBlox modules where "bad" data can exist.

OUTOFFn—this line connects to the MUTEn input of the output connector modules and would normally operate a relay (or equivalent) that shorts the (analog) output lines to ground.

Some carriers may allow selectable jumpering and routing of MUTEn and OUTOFFn signals so the guidance here may not match a specific hardware configuration.

FAULTn—Indicates a module is in a very unhappy state. Really only for DigitalBlox systems; an analog only module in an unhappy state is probably emitting smoke and flames and a digital level won't help.

DIGPOWERn, **ANAPOWERn**— connects directly to the corresponding control pin on the supply connectors. Pull low to enable the respective supplies. Normal sequencing rules would imply digital first. Details are a function of the supply actually used.

RESETn—connects to all modules. Good idea to have previously asserted MUTE before playing with reset.

POWERGOOD—sourced by the power supply, this signal indicates that primary power is available. If the system is running and this signal is de-asserted (low) then the host processor has only the hold up time of the supply to safely mute the outputs to avoid possible output anomalies on analog outputs.

On power up supplies may delay this signal to give their regulators time to stabilize, but this signal is not intended to be a supply output watchdog.

SYNC, TC—These signals are routed on DigitalBlox carriers to provide a way to offer sample accurate synchronization. Using the same I2S MCLK and Frame Sync ensures samples are aligned but does not ensure specific samples are aligned across multi-node systems.

The exact implementation of the SYNC and TC signals is a function of the processor device(s) used. Typically SYNC may transition every 256 samples and the TC carries the frame count of that transition, but details are implementation specific. A^2B based signal transport handle this issue by design, it's only an issue if using I^2S for data transport in multiprocessor systems needing absolute timing across all I/O.

© 2020 **Clockworks Signal Processing LLC**

Signal Processing

DigitalBlox®

Signal and design summary

DigitalBlox modules use a 40 pin connector for I/O. The upper 20 pins carry I2S audio and related signals; the function of the lower 20 pins depends on if the connector is an input or an output connector.

ADC modules have an analog input and digital output connector, DACs are reversed with a digital input and analog output connector.

This guide will use the term *DSP module* to mean the module that sits between the ADC and DAC modules regardless of the exact function/ features implemented there.

In the first version of the SignalBlox architecture a number of digital signals are being left as expansion/enhanced features for later systems. The use of these signals is dependent on the carrier board and the modules connected to them and there is no prohibition against using them now. We don't suggest using them for a different purpose as that will create compatibility issues with future SignalBlox systems.

Input side connector

signal	pin	pin	signal
+5	1	2	+3.3
GND	3	4	GND
SDA	5	6	SCL
RESET_INn	7	8	INTn
GND	9	10	GND
SYNC	11	12	TC
GND	13	14	GND
USB D+	15	16	USB D-
GND	17	18	GND
USERD1	19	20	USERD2
MUTE_INn	21	22	GND
FCLK_IN	23	24	GND
MCLK_IN	25	26	GND
BCLK_IN	27	28	GND
GND	29	30	D0_IN
D1_IN	31	32	D2_IN
D4_IN	33	34	GND
GND	35	36	D5_IN
D6_IN	37	38	D7_IN
D7_IN	39	40	GND

Output side connector

signal	pin	pin	signal
+5	1	2	+3.3
GND	3	4	GND
ADDR0	5	6	ADDR1
RESET_OUTn	7	8	FAULTn
GND	9	10	GND
MISO_1	11	12	MOSI_1
GND	13	14	GND
SCK_1	15	16	SSEL_1
GND	17	18	GND
UART_TX	19	20	UART_RX
MUTE_OUTn	21	22	GND
FCLK_OUT	23	24	GND
MCLK_OUT	25	26	GND
BCLK_OUT	27	28	GND
GND	29	30	D0_OUT
D1_OUT	31	32	D3_OUT
D4_OUT	33	34	GND
GND	35	36	D5_OUT
D6_OUT	37	38	D7_OUT
D7_OUT	39	40	GND

© 2020 **Clockworks Signal Processing LLC**

Digital Connector I2S signals

The upper 20 pins of the 40 pin digital connectors serve the same basic purpose on both the input and output. I^2S signaling normally follows the Philips Semiconductor convention (MSB to LSB, 24 or 32 bit, MSB starts one BCLK after FCLK); however source and sink devices can operate in any agreed upon mode they support.

MCLK— Master clock. Usually operates at 128x times the sampling rate but some systems may need 256x or 512x. Some ADCs and DACs have an internal PLL and do not require this signal.

In most cases MCLK is common across an entire system. One node in the system is the clock master (which includes the bit and frame clocks) and all other nodes are clock slaves.

Generally the carrier has responsibility to define the clock master and/or provide interconnect between places. However things like A2B bus provide an alternate way for accurate time alignment across systems versus routing the three I^2S clock lines to everything.

BCLK—Bit clock. This is the clock used to clock the data. Data is clocked in in the opposite edge that it is clocked out on, which usually means the relationship between this clock and the data can be a bit sloppy. However as with MCLK and the frame clock, it is important for clean edges and therefor most hardware buffers and redrives all 3 clock related signals.

In a very deep clock tree this extra buffering's effect on setup time as well as accumulated jitter must be considered. In the case of TDM data on the I^2S (i.e. 4 or 8 channels per I^2S data line) the bit times are correspondingly shorter.

FCLK—Frame clock, though many I^2S systems refer to this as frame sync. For 2 channels per I^2S line the FCLK line is usually 50% duty cycle and can be thought of as a clock. For higher channel count TDM the FCLK signal is usually just active for the first channel and therefor not a clock, in some cases it is only active for one bit period. In all cases this signal operates at the sample rate and serves to make sure all ADC and DAC devices are in phase with each other for their sample acquisition time.

D0-3—Primary I^2S signals. In standard I^2S this provides 8 serial audio channels, usually 24 or 32 bit. In the case of TDM4 only D0 and D1 are used, and for TDM8 only D0 is used.

D4-8– Secondary I^2S. Used for double density system (16 channels/module).

MUTE_INn— Module input connector only: indicates the upstream device does not have valid (I^2S) data. This might apply if the ADC has clipping detection (see FAULTn). If it's a SPDIF Rx, would indicate loss

of lock/valid data. Systems probably want to gracefully MUTE on any affected channels in this scenario.

MUTE_OUTn— Indicates that any connected DAC should enter its MUTE state and most likely propagate the MUTE state to any other analog modules. This signal most likely should not cause the output connector module to MUTE as those are generally a hard MUTE for avoiding clicks/pops during system power cycle. Details of how MUTE is treated are defined by the carrier board(s).

Digital input connector signals on pins 1-20

SDA, SCL, INTn— I^2C control for the module. INTn is an OC signal that module can use to indicate that the host should read the module status.

RESET_INn— Used to reset the module. This only applies to DSP and DAC modules. The system host controller operates this signal line; if the controller is actually installed in the DSP

Use of this signal by DSP and DAC modules also has implications for data buffer synchronization. The I^2S clock signals ensure the correct phase relationships across the hardware but do not solve the issue of ensuring devices with buffers (e.g. DSP chips) all align their buffers correctly.

DAC modules should MUTE their output in the reset state, as well as assert their own MUTE output to any analog modules connected to them.

ADCs receive their RESET signal from their input side but may also allow jumpering of the (normal output) to the control side as a way to give DSP direct reset control of the ADC. This type of non-standard use case is system dependent.

SYNC, TC—These signal lines are planned for a later phase of SignalBlox implementations to support use cases where a global sync and time code are required.

USB D+/- - Some modules may require a USB interface to control them (as a USB device) or in the case of the DSP modules may need to implement USB host features for control. Carrier board designs consider this interface optional.

USERD1, 2—Carrier boards route these signals to an unpopulated header. They're intended to provide a way to add wires for hacking a prototype without running wires between a module and carrier.

Digital output connector signals on pins 1-20

ADDR 0,1—These can be used by the DSP module (and the DAC module if needed) to know their position on the carrier card. Typically the lowest address card (00) would be the clock master for the carrier. As each module location can be addressed uniquely via addressable I2C muxes these signals would normally not affect I^2C address use.

RESET_OUTn— In the case of the DSP module digital output connector this is used to reset the downstream DAC in that section. As with the RESET input, consideration for buffer synchronization across multiple DSP sections must be considered.

FAULTn—Indicates a problem with the module. Normally carriers route this signal to a register where it can be read under host control. It may also be jumpered to the analog output connector hard output MUTE signal. The MUTE_OUT signal is used to set downstream devices to the MUTE state, though it's probably a good idea for an actual fault to cause a MUTE.

ADC outputs normally can not fail, this signal can however indicate clipping which may require further system action to minimize audible problems.

MISO, MOSI, SCK, SSEL—SPI slave interface. Some DSP modules may only be operated via SPI. This is an optional feature for the carrier cards.

UART_TX, _RX—Some DSP modules may use a serial port as part of their interface, particularly if they include an ARM based processor. Carrier that implement this provide these as LVTTL level signals and would need an adapter for a RS232 connection. Each DSP module position must have its own serial connection as there's no flow control, i.e. the serial signals can not be multiplexed.

© 2020 **Clockworks Signal Processing LLC**

(this page intentionally blank)

FAQ

All of the things we guessed someone might ask about but nobody really cares about.

These things are huge, why isn't the hardware the size of a postage stamp so I can wear it on my wrist?

One of the primary goals of the SignalBlox system is to make it easy to modify the hardware if needed to match a specific prototyping need. After a long and detailed set of tradeoffs (otherwise known as a coin toss) it was decided that 2.54mm (.1") connectors have a lot of advantages to be able to easily modify the hardware as well as being the lowest cost connector style. Once that was established the module dimensions had a clear lower limit.

The second consideration is that these modules are intended for high channel counts, and if the system has 64 channels in and out it's not a physically small system.

The other sizing calculation was based on placing the needed hardware for the planned functions on the board without going to unique form factors.

But I'm developing a T shirt that plays 64 channel audio !

While we had certain reasons for making things the size they are, you may very well have different needs. We encourage you to take these designs and combine them to save space and use those 0.1mm pitch connectors instead (yeah we made that up).

Why are all those big 0805 resistors there— I'm going to use 0201 in my designs to save space!

Ignoring the manufacturing headaches that come with the small parts, for resistors in the analog signal path you want to stick to 0805 or larger parts as the small parts may exhibit high THD. Clockworks also almost always uses thin film parts in the audio path as thick film parts are, on average, noisier. You can read about that here: http://www.aes.org/e-lib/browse.cfm?elib=19750

Why aren't the headers on the carrier boards shrouded to keep them aligned?

Originally they were, but after playing with a few prototypes and using different brands of connectors we realized that there is simply no standard IDC/2.54mm connector. To deal with that most shrouds are vastly oversized, to the point where you can plug it together and be off by 1 row. And with a shroud you can't see you're off by one. It is true of course that the mounting holes won't line up, but nobody checks that when they're in a hurry.

IDC cable connectors are less of a problem as they have the center keying tab. However PCB mounted female connectors are not available with the center keying tab.

With unshrouded headers on the carrier boards you can see that things are not lined up.

Am I reading the drawings for the modules correctly, are the two connectors offset from each other?

Yes.

When the original concept had shrouded headers on the carrier then the offset would have made it even more difficult to plug a module in incorrectly. Without the shrouded headers the offset isn't as useful to avoiding mis-mating modules to carriers, but we left it there as we already had things designed and it doesn't hurt.

I want to modify some of the designs for my own use, do I have to publish everything?

While we would encourage you to share your ideas, if you are not providing your work to anyone else then there is no obligation to publish it; for more about this topic see the background for the GPL license used for

open source software and the Creative Commons licenses.

If you do make a derived design available to others (i.e. you sell hardware either as a board or as part of a box level system) then you must follow the CC 4.0 SA-BY license rules and provide the design files of any design based on the ones provided to anyone who requests it. You do not need to provide designs of other hardware you designed independently.

We are not currently licensing under the OSHWA license as only the design files are subject to license, hardware itself can not be copyrighted and there are no patents on the SignalBlox designs. The licensing terms may change in the future.

I modified something and now it doesn't work. What are my options?

As the modular nature limits the amount of circuitry, the best step is to test just your modified design in isolation from everything else. Generally a test fixture of some sort for each module design is required.

If you're still stuck then we suggest asking question on the Clockworks forum or whatever your favorite place to turn for help is.

Clockworks offers support for supporting modified hardware on a paid basis only.

How does that volume control module work with balanced signals?

This is a little unconventional as normally volume controls are single ended. However some experimentation showed that using two channels of the NJR part (one for "+", the other for "-") actually works well and avoids the input and output conversion stages for a system with balanced in and out - with the caveat that the balanced input signal should have low common mode noise levels. If it's connecting to the outside world this is probably not the case and a balanced buffer stage should be used to eliminate the common mode noise on the input.

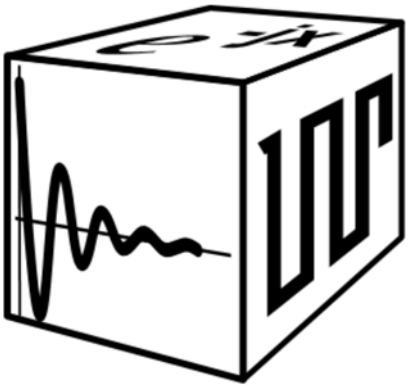
What about grounding?

This is a complex question that could fill a book. Within the SignalBlox system there is just one ground for everything. On carriers this means that there is a dedicated ground plane and generally all other layers flood ground plane. The same applies to modules, though with 2 layer modules there are sometime limited traces on the bottom (ground) side.

The I/O modules are grounded to the carrier board through the ribbon cables, which have a liberal number of ground wires to minimize impedances as well as loop area for return currents.

Despite the attention paid to grounding in the design as soon as a system is connected to the outside world all bets are off about electrical noise making it in to the signal path as well as potential EMC/EMI issues. Proper enclosure construction and good connection of connector shields are critical to overall system noise performance. The mounting holes of the boards are connected to ground plane and can be used for attaching supplemental ground connections. In other cases using nylon hardware for mounting may offer benefits. You should be prepared for some experimentation as there is no one size fits all solution.

CLOCKWORKS
Signal Processing



SIGNALBLOX®

OPEN SOURCE MODULAR HARDWARE FOR SIGNAL PROCESSING

HTTP://CLK.WORKS

info@clk.works

+1 978 258 5402

© 2020 **Clockworks Signal Processing LLC**