

# TECHNOTE 007

## SPICE SIMULATION OF A<sup>2</sup>B

Guide to LTspice files for A<sup>2</sup>B analog simulation

Rev 1.0

28-April-20



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## 1 INTRODUCTION

As part of an investigation in to A<sup>2</sup>B operation for a technical article a number of models were created in LTspice to compare against measurements and help understand how the parts in the suggested Analog Device's design work together.

The files are available from the Clockworks website: <https://clk.works/2020/04/ltspace-files-for-a2b-simulation/>

This Technote discusses the assumptions made in developing the LTspice model. The circuit design is based on ADI's guidance from the document *AD241X, AD242X, Reference Schematics Rev 2.1, August 9, 2019*, (A2B-Reference-Schematics-Rev2.1-2019-08-09.pdf) available from ADI's website.

As others may be interested with understanding the design or modifying it for different applications the source files have been made available for others to play with. If you discover something interesting (or mistakes) please let us know.

### 1.1 USING THE FILES

The schematics were created with LTspice XVII, available from ADI's website.

The schematics use the detailed part model for the TDK common mode choke. It's not redistributed in the download, please get the precision model from:

[https://product.tdk.com/en/search/emc/emc/cmfc\\_cmc/info?part\\_no=ACT1210L-101-2P-TL00](https://product.tdk.com/en/search/emc/emc/cmfc_cmc/info?part_no=ACT1210L-101-2P-TL00)

Note the TDK model and the default LTspice create symbol put the pins in a funny order that you will need to fix.

There is also a TDK 180 nH inductor used in one of the test files, the precision model is available from [https://product.tdk.com/en/search/inductor/inductor/smd/info?part\\_no=MLG1005SR18JTD25](https://product.tdk.com/en/search/inductor/inductor/smd/info?part_no=MLG1005SR18JTD25).

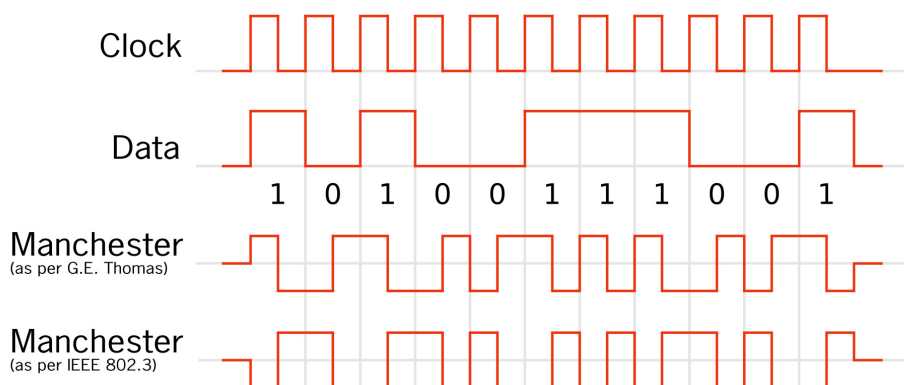
### 1.2 NO PROMISES...

The explanations are the authors opinion from reverse engineering the system and or experimentation with LTspice. Chance of an oops being there is > zero.

The document will be updated if new/better information is obtained.

## 2 MANCHESTER ENCODED DATA

The ADI A<sup>2</sup>B parts use Manchester coded data, where a zero is indicated by a falling edge and a one is indicated by a rising edge (802.3 version, not conclusively verified).



**Figure 1** Illustration from [https://en.wikipedia.org/wiki/Manchester\\_code](https://en.wikipedia.org/wiki/Manchester_code). (figure by user [Loopkid](#), public domain)

The SPICE analysis include AC analysis, i.e. magnitude vs. frequency plots of the response, it's helpful to remember that this is not the same as the actual spectrum at that point, as Manchester encoding creates a specific spectral pattern.

This set of lecture notes explains how to derive the spectrum:

[http://www.siu.edu/~yadwang/ECE375\\_Lec8.pdf](http://www.siu.edu/~yadwang/ECE375_Lec8.pdf)

As 10BaseT uses Manchester encoding (10 Mbps instead of 49.152 Mbps for A<sup>2</sup>B) we can get a sense for the spectral shape from the information published by the IEEE. For example see [http://www.ieee802.org/3/cg/public/Nov2017/An\\_3cg\\_01\\_1117.pdf](http://www.ieee802.org/3/cg/public/Nov2017/An_3cg_01_1117.pdf). Figure 2 is copied from the that document (page 7). Frequency axis should be multiple by (approximately) 5 for A<sup>2</sup>B spectrum. The data spectrum will have a natural minima at twice the data rate; square waves only have odd harmonics so all of the even harmonics are ideally zero.

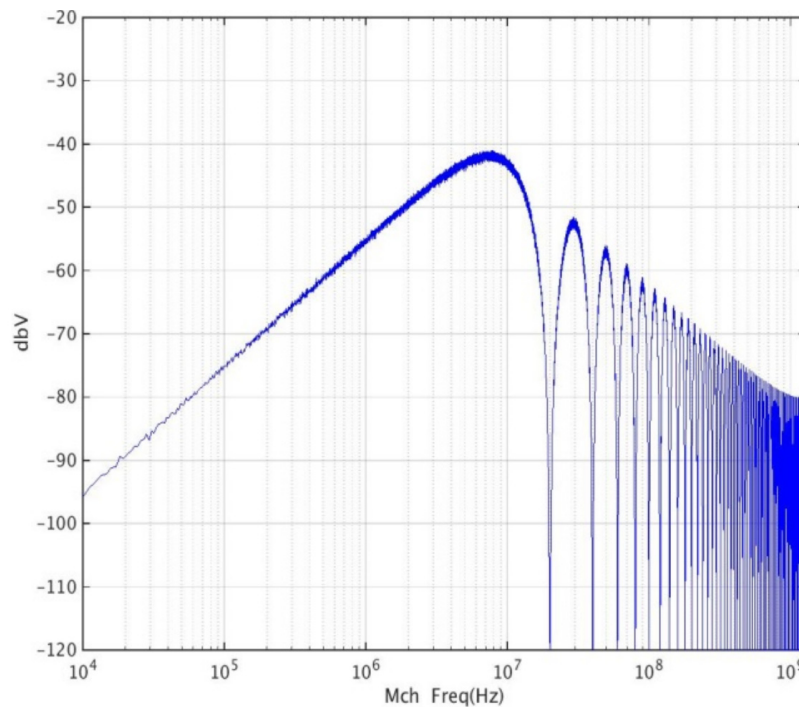


Figure 2 Manchester encoded data for IEEE802.3 10 Mbps data, see text for credit.

The actual A<sup>2</sup>B spectrum is more complicated because data is only encoded and sent when needed, there's no continuous clock with zero data. This creates 48 kHz period to the data bursts, however since we're really just interested in the active data portions and the effect of the ADI recommended circuits on them we can overlook the extra complication from A<sup>2</sup>B's burst nature.

### 3 CABLE MODELS

LTspice lacks a built in detailed CAT5 twisted pair cable model for use with differential signals. Knowing R, L, and C per meter we can use the lossy transmission lines (LTRA) create something that comes close.

While investigating twisted pair cable models for SPICE some descriptions imply the models only put inductors in the "top" line and the second line is just a straight through connection intended to be grounded, like one would do with coax. At least in the case of LTspice the LTRA model does not operate like that.

This simple model also seems reasonable because A<sup>2</sup>B default of unshielded twisted pair (UTP) is the simplest configuration, i.e. there's no shield and no other cables pairs. With A<sup>2</sup>B's generally lower frequencies we don't need to have a more accurate model that accounts for the fact that the cable's L, C, and R are slightly frequency dependent.

## 4 FM/DAB FILTER

Based on the labeling of the parts in the ADI's schematic reference document it's assumed that these parts were added to lessen the interference in the broadcast bands. The A<sup>2</sup>B signal spectrum has a natural null at twice the 49.152 Mbits/sec data rate at 98.3 MHz. Since links are bidirectional the filter is replicated on both ends.

The schematic is in `FM_DAB_bal_filter.asc` and contains 3 different sections to allow comparing results for the following cases:

- Standard inductor (180 nH) with parasitic  $R_s$ ,  $R_p$ , and  $C$ .
- Precision TDK model for the recommended 180 nH part.
- Standard inductor (180 nH) with parasitic  $R_s$ ,  $R_p$ , and  $C$  and additional low frequency filter (3.3 $\mu$ H + 0.33 $\mu$ F)

The 3<sup>rd</sup> case appears in some of the suggested ADI circuit configurations, though it's not clear what the intended purpose is. It only appears in local powered slaves and is not present phantom powered slaves.

The capacitors and resistors do not use any parasitic values in the LTspice files.

Figure 3 shows the schematic used, and Figure 4 the results of the three different circuits AC analysis, along with a zoomed in view shown in Figure 5 to show the very slight difference between the first two cases.

Figure 6 shows the filter's effect in the time domain. These are potted as the differential voltages. The 3<sup>rd</sup> case is shifted due the high pass filter (3.3 $\mu$ H and 0.33  $\mu$ F); note the time shift in the `.tran` command to let that start to stabilize before plotting.

These tests were only looking at the model differences; in the real system this filter is important for the A<sup>2</sup>B port when it's driving and here we're only looking at the effect on the receive side. The driving source here is not the same as having it driven by the actual design; the later models are for that.

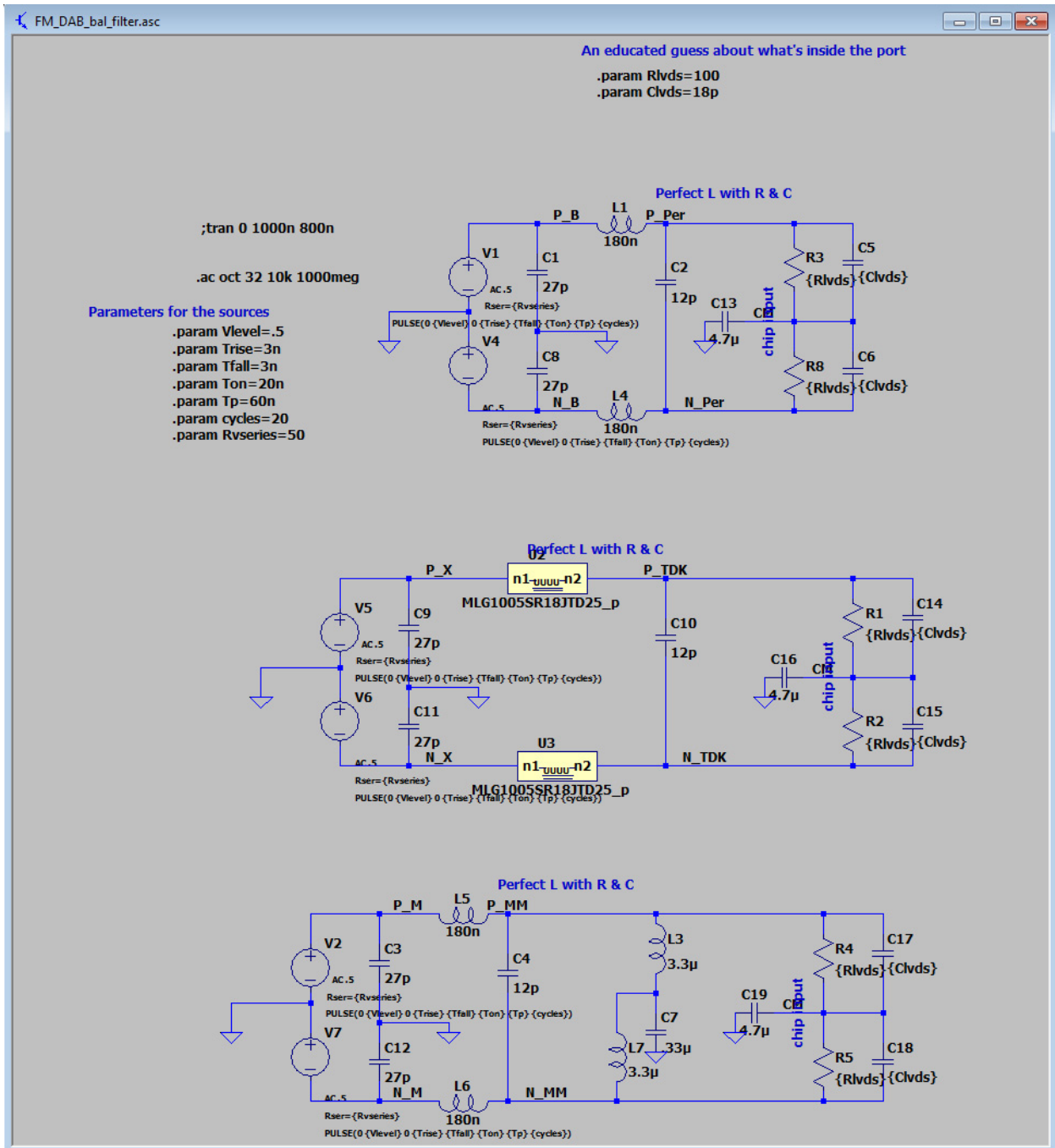


Figure 3 FM/DAB filter simulation schematic



Figure 4 Comparison of the 3 models. Green with simple inductor, Blue with the precision TDK model, and simple models with the extra filter section.

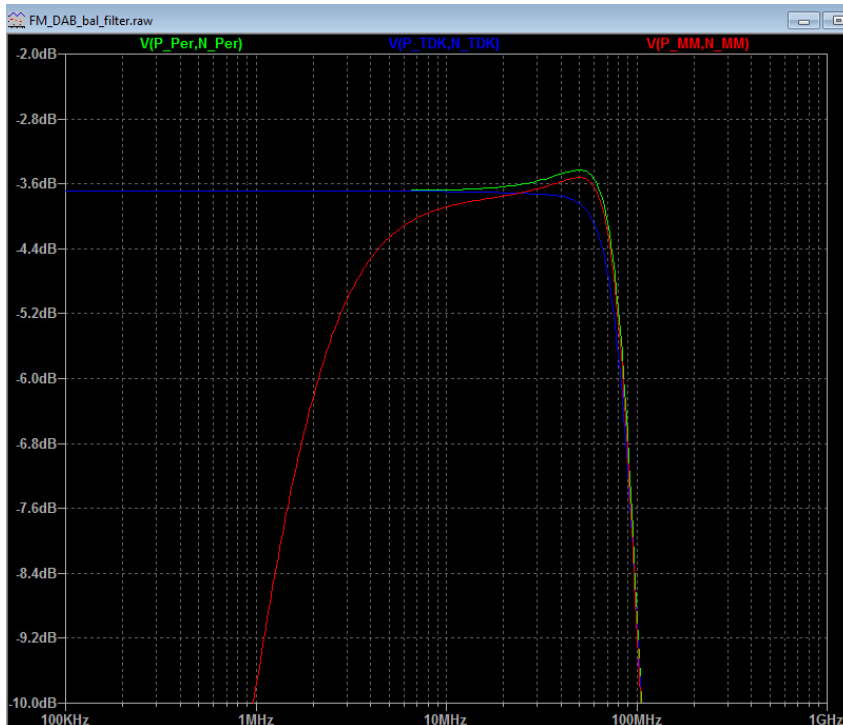


Figure 5 Zoomed in view of prior traces showing slight difference between the precision 180 nH inductor model and the simple built in part with parasitics added





Figure 6 Time domain view of pulse waveform similar to A<sup>2</sup>B data.

## 5 INPUT SECTION MODEL

This model, in the file `A2B.input.network.asc`, builds on the prior one and adds the rest of the components between the input and the transceiver. It uses the circuitry ADI defines for a local powered slave. Figure 7

There's probably not much of interest with this one, it was used to confirm that the models for the different sections were giving reasonable results before creating the full end to end version.

As with the prior section, the driving source is not an A<sup>2</sup>B transmitter so the actual waveforms would look different than those observed with this model.

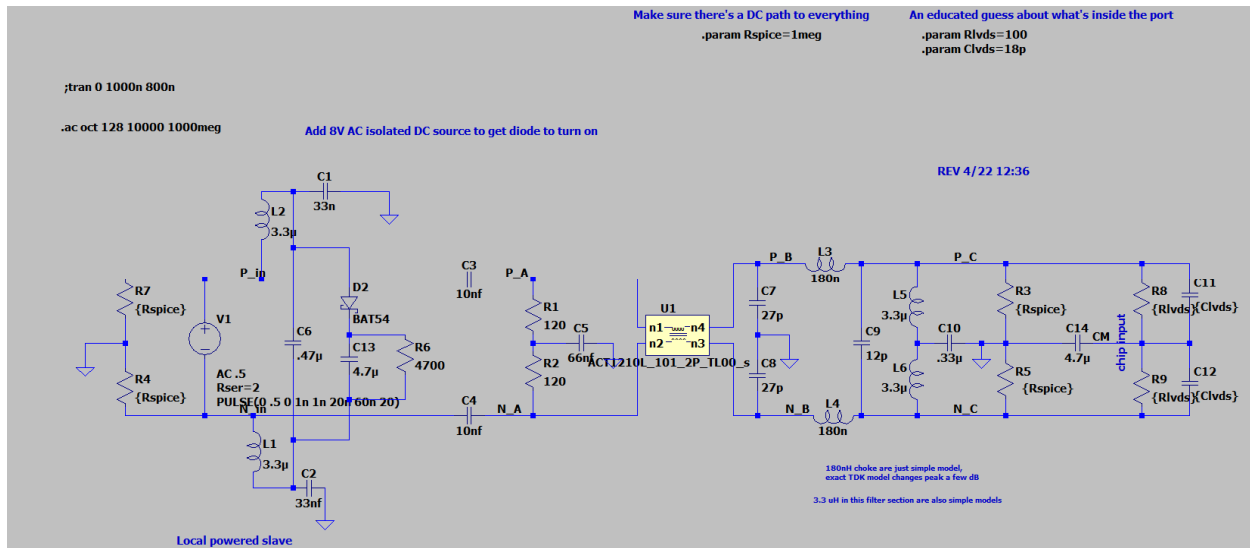


Figure 7 Local powered slave.

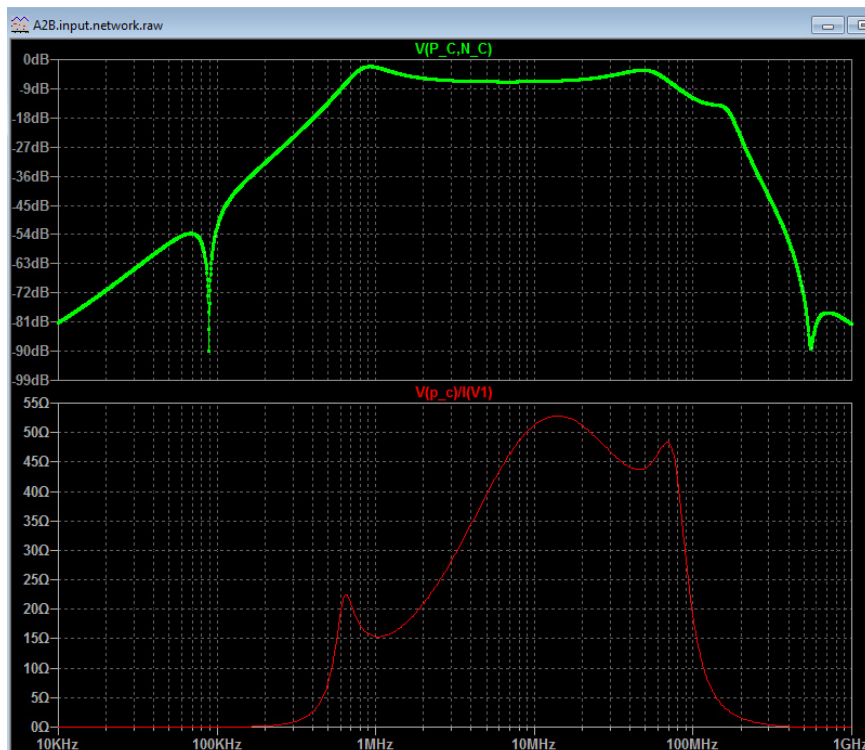


Figure 8 AC simulation result. Input to chip input response (top trace) and input impedance (single ended, double for differential value).

Of interest was the frequency response (top plot in Figure 8) and the impedance. The impedance was of interest since at first glance the termination looks "all wrong" but we can see that across the

frequency range of interested (10 MHz to around 90 MHz) it generally hovers around 50 ohms (single ended).

## 6 OUTPUT SECTION MODEL

There's no difference between "output" and "input" since operation is bidirectional. It is easier to have two different schematics to simulate to get an idea how the two sides are behaving.

The file for this is `A2B.output.network.asc`. It's the same as the one in the previous section except the signal source is now on the right side and represents the A<sup>2</sup>B transceiver, Figure 9. The transmit side is modeled as a current source to make the effect of the internal 100 ohm resistors that are also there for termination in the receive mode a bit more obvious.

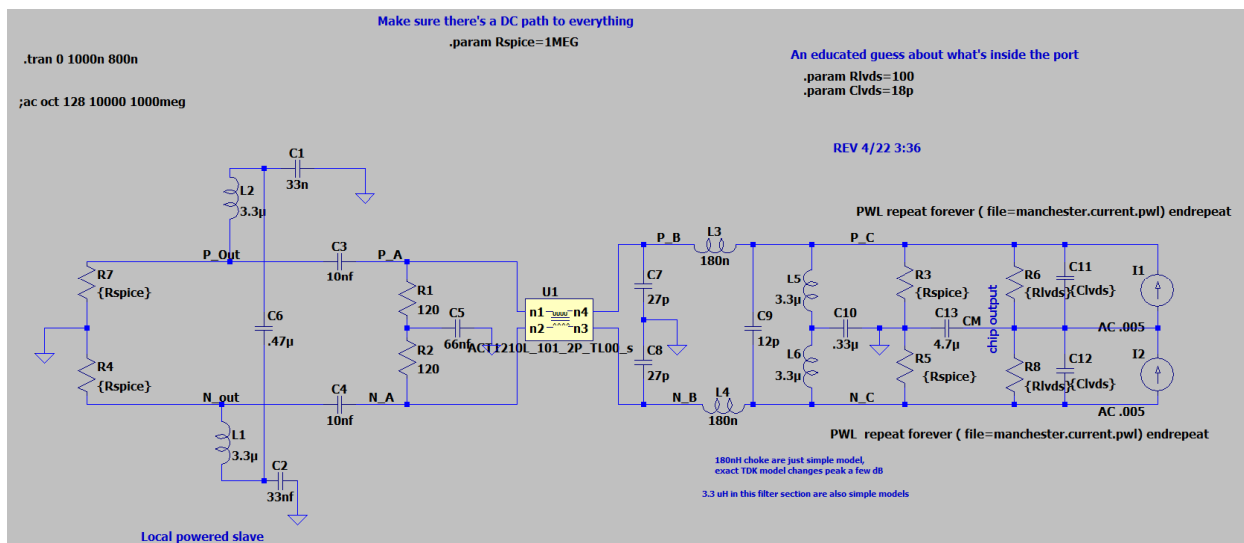


Figure 9 Output schematic

Another difference is the current sources are using a file to create a waveform that corresponds to a short Manchester encoded data stream as this will give us a crude spectrum (Figure 12 of the actual A<sup>2</sup>B signal that is output and not just the frequency response of the filter functions. We can then compare this against actual spectrum captures (they pass the eyeball test).

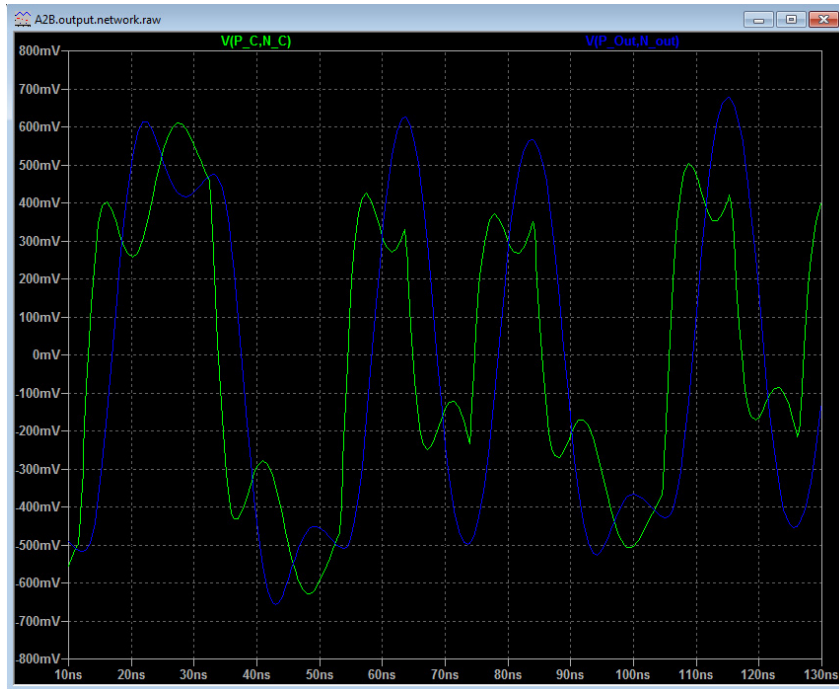


Figure 10 The chip output (Green trace) is affected by the FM filter so does not show clean edges. The blue trace is the output at the connector, though there's no load so actual system response would look different.



Figure 11 Frequency response plots at same places as waveforms in Figure 10

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Figure 11 shows the frequency response of the system at the IC's outputs (which is loaded by the filter) and at the output.

The AD2428 has the capability for reduced drive strength and this will change the levels; it is assumed that the impedance of the chip's output does not change with different drive levels.



Figure 12 Output spectrum using a short simulated length of Manchester encoded data. A more detailed/longer run would be needed to get an overall smooth spectrum.

## 7 FULL END TO END MODEL

Once the input and output models were created and tested they were connected up with a simulated piece of CAT5 UTP. The file `A2B.end.to.end.network.r2.asc` contains the schematic of Figure 13.

This combines the schematics previously investigated.

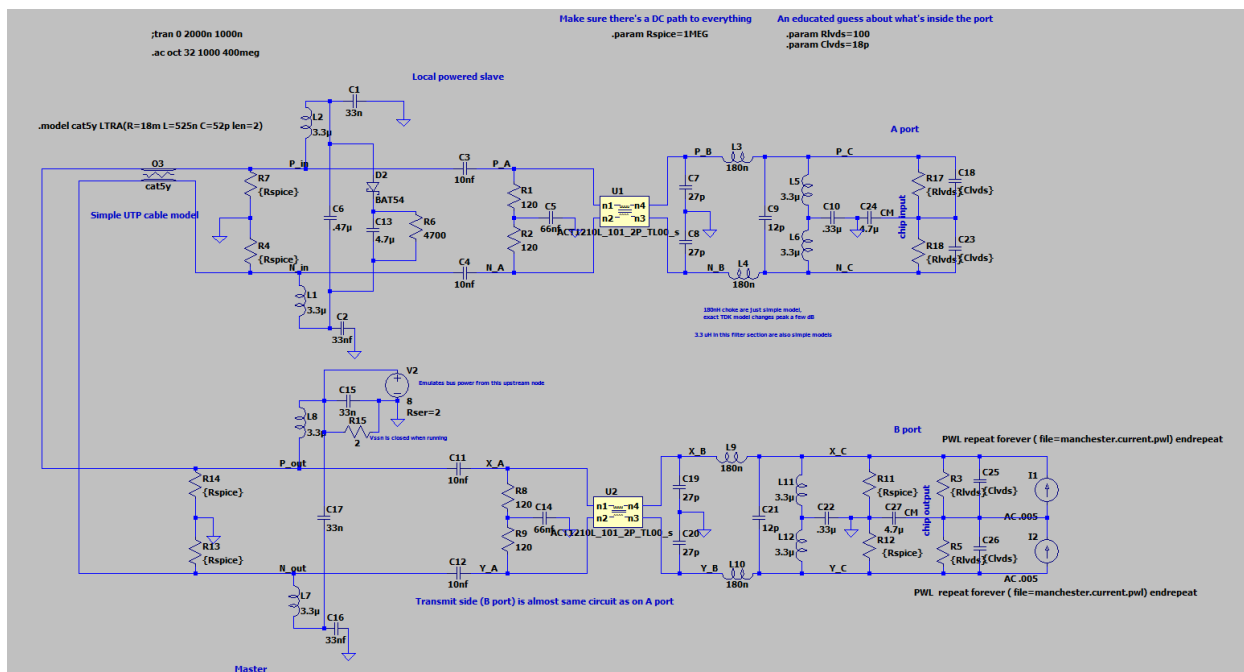


Figure 13 Full B port Tx to A port RX simulation model with 2m of CAT5.

Figure 14 shows the LTspice AC analysis results at various points in the circuit. As explained in Section 2 this is not the same as the spectrum of the signal that would appear at that point in the signal path as the Manchester encoded data has a specific spectral shape as well.

Figure 15 shows the LTspice waveforms at the connector for simulated Manchester encoded data. Figure 16 shows the actual measurement.<sup>1</sup> The scope/probe bandwidth as about 200 MHz; the A<sup>2</sup>B system response is well attenuated above 150 MHz so we don't lose much details with the selected scope/probe bandwidth.

A final comparison between the models and measurements is the A<sup>2</sup>B is the spectrum of the signal captured at the connector of the A port<sup>2</sup> as shown in Figure 17. The peak is at the expected (approx.) 50 MHz and 3<sup>rd</sup> harmonic at 150 MHz. The spike close to 100 MHz is actually a nearby FM station and illustrates the importance of knowing your test tools and system, otherwise one might assume in this case there's some sort of bad 2x clock signal ending up on the wire.

<sup>1</sup> Obtained with two probes and using the scope's match function to show the differential value.

<sup>2</sup> Captured/calculated just from V(P\_in) as the scope's math functions can not be nested.

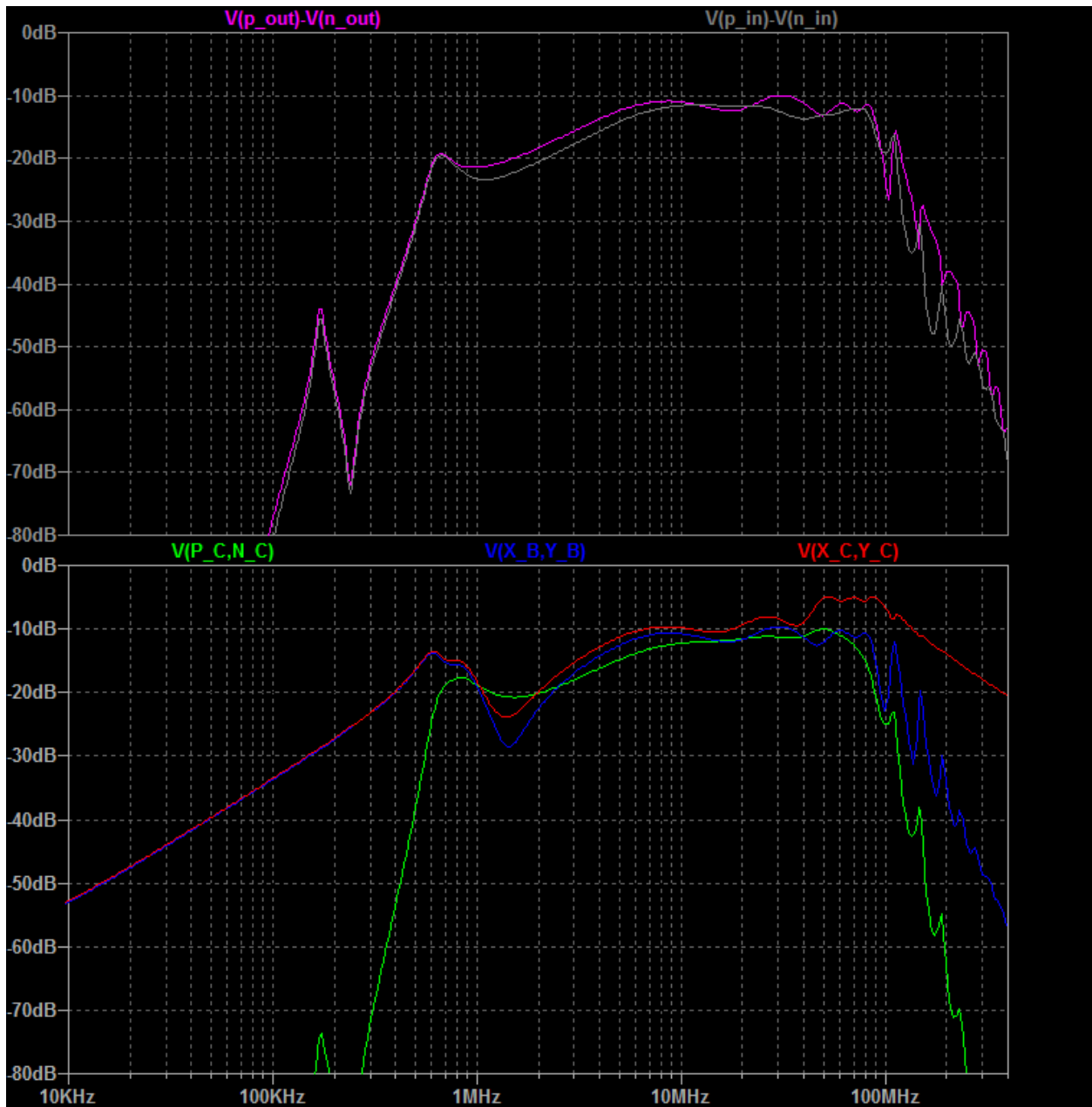


Figure 14 AC analysis plots from end to end simulation.

Top plot: Purple - output connector of B port, Grey – input connector of A port

Bottom plot: Red – chip out, Blue – FM filter out, Green – A port chip input

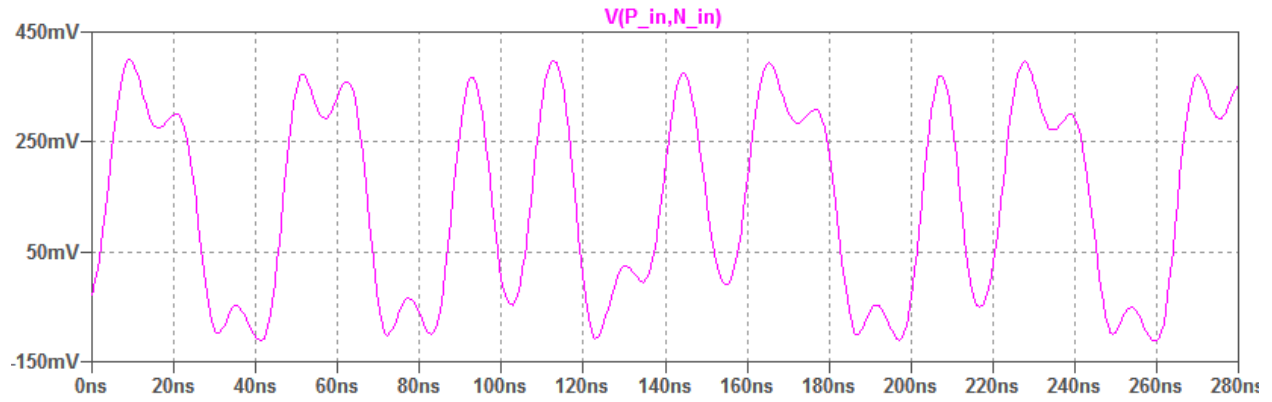


Figure 15 LTSpice simulation of input to A port at connector of Figure 13.  $V(P_{in}) - V(N_{in})$

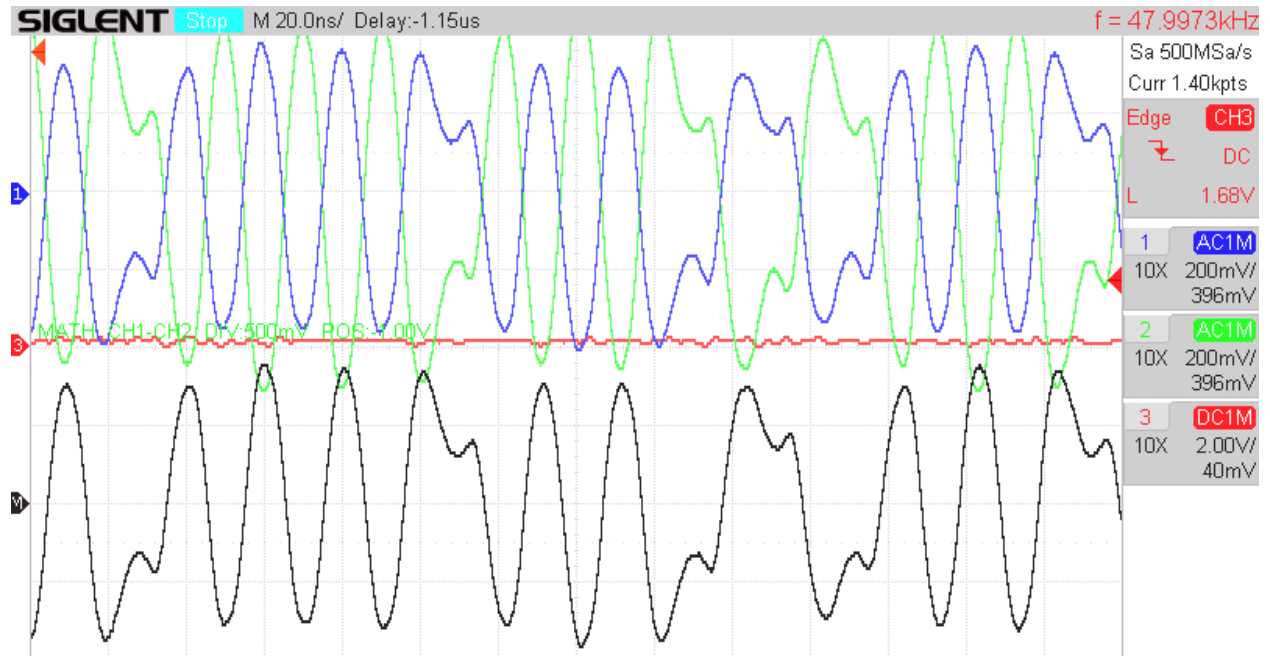
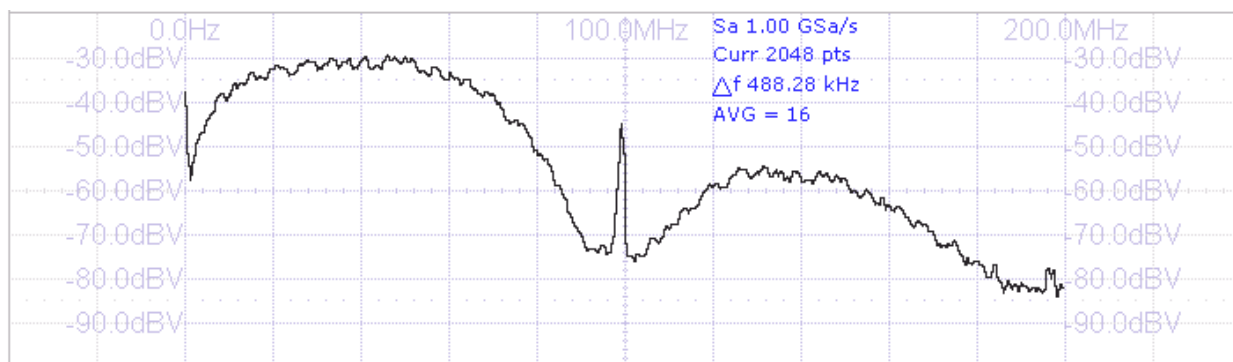


Figure 16 A<sup>2</sup>B data (black trace) computed from the captured P (Blue) and N (Green) signal lines at the connector. (Approx 200 MHz BW)





**Figure 17 Measured A<sup>2</sup>B spectrum (random data). Spike at 99.5 MHz is a nearby FM transmitter. Linear frequency scale.**

## 8 SUMMARY

The testing of the LTspice models showed that they behave reasonably in the frequency range of interest for A<sup>2</sup>B using basic component models with first order parasitic values. The one exception is the common mode choke, it was easier to just use the precision model and not worry about it.

The model is helpful in understanding what the design is doing and could serve as the basis for what-if analysis for applications that might have different needs. The ADI design is intended for use where the electronics and cable are unshielded and EMC requirements are more stringent than typical FCC/CE.

There are questions raised by the ADI suggested design that are not answered here:

- Importance of the FM/DAB filter section
- Reason for the 3.3μH/0.33 μF section on local powered nodes
- Benefit of the common mode choke<sup>3</sup>
- Why the split termination scheme
- Impact on ESD survivability with a different design<sup>4</sup>

<sup>3</sup> To be fair the model could be modified to add common mode noise and the impact evaluated, though without a clear model for the AD2428 input's CMRR across operating frequencies not a lot of insight would be gained.

<sup>4</sup> Somewhat like the common mode choke question, this could be simulated, but we don't know enough details about the AD2428 input port to include that in the model to decide if the device might be damaged.