TECHNOTE 008

A²B I²S CLOCK JITTER

Rev 2

5-July-20

Clockworks Signal Processing

http://clk.works/

1. TABLE OF CONTENTS

TechNote008 investigates the jitter properties of the I²S clock output of the AD2428 A²B transceiver part. Designers of voice grade and low end consumer audio products can probably cross this topic off of their lists. Designers of mid range and above consumer audio, and all pro audio applications, as well as related industrial, scientific, and sensing applications that need highly accurate ADC and DAC performance should continue on.

The AD242x A²B transceiver device's output clocks have high jitter in comparison to I²S clocks derived from crystal oscillators that are typical in most ADC/DAC systems. The performance effects of the A²B transceiver clock output jitter may not be of that much concern if the ADC and DAC have excellent internal PLL stages.

This TechNote and the associated support materials are intended to provide designers a general framework for their own testing to gain information beyond what can be found in typical part's datasheet.

1 INTRODUCTION

In testing Clockworks' ADC and DAC board prototypes that are part of the SignalBlox system, a configuration using A²B for data transport was the first one tried. Further details of the hardware are available on the Clockworks website.

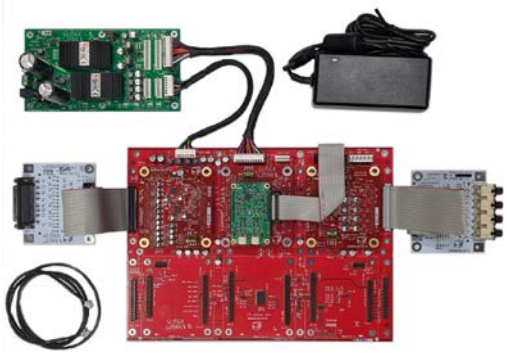

Figure 1 Clockworks 8 channel ADC and DAC with A²B interface initially used for test

During that testing what seemed like a very high noise floor, 10 dB higher than the worst case datasheet number, was measured on the ADAU1979 ADC. An investigation in to the cause was

started, and during that what looked like high I²S clock jitter was noted. At about the same time the cause of the high noise floor was realized to be pilot error in making the noise floor measurements. The revised value just fell inside of the worst case number DR number of 103 dB (versus 109 dB typical). System test moved on with a note to come back later to look at the clocks and see if that would explain the degraded noise floor.

Clock jitter specifications for the AD2428 A²B transceiver had been of concern on the Clockworks hardware because of this table in the datasheet:

Table 10. SYNC Output RMS TIE Jitter at Each Slave

Slave Node	Typ	Max	Unit
1	1.57		ns
2	1.79		ns
3	1.91		ns
4	2.04		ns
5	2.15		ns
6	2.27		ns
7	2.44		ns
8	2.47		ns
9	2.58		ns
10	2.70	5.50	ns

Figure 2 RMS TIE table from AD242x datasheet

tSOJ from the parameters in Table 7 of the AD2428 datasheet specify 2.2 nsec typical and is assumed to be an average derived from the above. Regardless, this is an unusually high number for audio designers.

For those not familiar with the topic of jitter and audio, or with an interest in the test setup that was used to measure the jitter, please see Clockworks Appnote001 – Jitter Spectrum measurement with a DSO. It provides a review of jitter measurement, jitter as it applies to audio, and a Python program and excel spreadsheets to reduce DSO data in to a form useable for analysis. This provides a jitter spectrum derived from the TIE (Time Interval Error) data so that the spectral shape of the jitter can be used to estimate the impact on signals.

That AppNote also establishes two criteria – one related to measurement (direct or indirect) of jitter such as an audio equipment reviewer or audio professionals might be concerned with, and the second is an audibility criteria.

1.1 TERMS

Here's the TL;DR for AppNote001 and its references:

- Period jitter. Measured clock period minus the ideal clock period
- Cycle-to-cycle jitter. Current clock period minus the previous clock period
- Time Interval Error (TIE). Time position of Nth clock edge vs. ideal Nth edge
- All three can be characterized by RMS or peak-peak values.
- Period and/or cycle-to-cycle jitter are usually of interest to processor and SERDES designers[1]
- The spectrum of TIE is of primary interest for audio designers, though low RMS and peak to peak values (10s or 100s of psec, respectively, across a relevant time window for audio) can generally mean it won't be an issue

Sometimes TIE is written as TIE jitter, but since the E stands for "Error from jitter" where jitter means all sources of error and not just random or noise ones it is technically redundant to say TIE jitter, sort of like saying A2B bus.

1.2 TYPICAL PERFORMANCE

Though it does not inform the reader about the audio performance, high quality audio products typical advertise period and cycle to cycle RMS jitter of less than 50 psec RMS. Peak to peak values are usually not advertised and the relationship between RMS and peak is in part determined by how the RMS was measured. Further complicating matters is the JEDEC standard for measuring jitter on highspeed SERDES interfaces as a way to estimate BER (Bit Error Rate) of an interface, but that methodology is not appropriate for ADC and DAC clock jitter, which need the consecutive edge to (ideal) edge measurements from measuring Time Interval Error (TIE) and calculating its spectrum.

TIE with strong spectral components, even with low RMS values, will show up in analog testing unless the ADC and DAC clock systems remove it.

A single number for RMS TIE is difficult to interpret for audio impact, though it can be generally assumed that if the TIE RMS value is on the order of few tens of psec or less, the system's jitter

[1] These terms are copied from ADI's EE-261 https://www.analog.com/media/en/technical-documentation/application-notes/EE-261.pdf

will probably not have any adverse effects on either audibility nor measurements that expose clock jitter.[2]

The opposite it not true, a high (greater than say 100 psec) RMS TIE does not automatically mean the system will have bad audio performance; performance can only be determined from actual testing. The AD2428's datasheet value on worst case RMS TIE of 5 nsec is 50 times greater than the criteria that Clockworks would normally use.

1.2.1 SYSTEM PERFORMANCE IMPACT

Complicating matters is that ADCs and DACs all respond to clock jitter differently, and theoretical analysis is difficult. With pro audio aiming for Dynamic Range (DR) > 120 dB (AES-17 measurement) and consumer systems having DR > 110 dB, system measurement and test is the only definitive way to evaluate the impact. By design freeze a problem could involve significant redesign so prototypes should be fully vetted before committing to a design.

The reader is referred to Clockworks Appnote001 – Jitter Spectrum measurement with a DSO for more details.

2 TEST CONFIGURATION

A three node configuration was used:

- Master node: Analog Devices EVAL-AD2428WD1BZ (operated as master, controlled via USBi from PC with SigmaStudio)
- First slave node: Analog Devices EVAL-AD2428WC1BZ (4 channel PDM microphone)
- Second slave node: Clockworks EVMA2B01 (EVM board for AD2428 expansion module, similar in functionality to ADI 'WBZ board)
- 1m long cables were used for interconnect between the three boards.
- All spread spectrum clocking features were turned off.
- Siglent SDS1204X-E scope. 200 MHz 1 Gs/sec[3]

[2] *Probably* is a vague term for engineering use, but appropriate here because there are too many variables and pathological cases to come out with a blanket statement, particularly when the ADC or DAC is generally a black box for handling clock jitter. The only way to know is to test.
[3] The maximum sample rate and the limited ENOB of the scope will contribute to these numbers being larger than the actual timebase stability of the scope, which if we assume is a reasonable

- Measured timebase stability and noise impact on measurements, 1 msec measurement window, 1 Gs/sec:
  - Period jitter 12 psec RMS, 62 psec peak-peak
  - Cycle-to-cycle jitter 7 psec RMS, 111 psec peak to peak
  - TIE 200 psec RMS, TIE 321 psec peak to peak[4]

The test location is subject to strong interference from a nearby FM broadcast station at 99.5 MHz.

2.1 RESOURCES

Clockworks AppNote001 includes a background section that provides references to relevant sources for jitter measurement as well as spectral analysis. Some additional resources on spectral analysis that are assumed in this document:

- Stefan Scholl, *Exact Signal Measurements using FFT Analysis* : good refresher on the topic
- Fred Harris, *On the Use of Windows for Harmonic Analysis With the Discrete Fourier Transform* : The 1978 paper most others refer back to.
- Wang Hongwei, Evaluation of Various Window Functions using Multi-Instrument : A list of more 'modern' window functions, with all of their performance information (but remember to convert to dB!)

2.2 DISTORT SOFTWARE

DISTORT is used to create a plot of the spectrum of a signal after distorting it in a number of ways, including jitter. Unless noted otherwise it was operated in the following fashion to produce the data presented here.

Using a small FFT (4096 points) makes it relatively easy to estimate the noise floor from the plot. DISTORT does not have a built in SNR measurement, and while data could be exported for analysis it would be a rather involved process. DISTORT does have a THD+N calculator, and when the jitter components are not harmonic this would be equivalent to the noise floor, though it was noted that the display value is -0.8 dB below the level set in the additive noise control.

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oscillator will have much better performance. These values are an order of magnitude better than the A²B hardware being measured so will not degrade the measurements..

[4] From Clockworks AppNote001. TIE peak to peak value can become unbounded over large measurement windows, and the spectrum is of primary interest anyway.

The FFT processing gain for 4K points is 33 dB. DISTORT offers a number of window functions, but the documentation does not explain the details on the window functions that have a parameter – typically called α that is included in the generating equation for the window function. The Blackman-Harris 7 term is an unambiguous choice in terms of the equation; it places the side lobes -180 dB down. The coherent gain is 5.7 dB but DISTORT already corrects for that[5]. The noise gain is 8.4 dB, so the RMS noise floor is 33 dB – 8.4 dB =24.6 dB higher than the "line" from displayed on DISTORT FFT spectrum plot.[6]

If the signal level was set to full scale then the noise being added would lead to clipping in the program as it treats 0 dBFS as the maximum. To avoid that signal levels are set to -1 dBFS, this will lower the effects of jitter a little.

For the purposes of simulating signals to gain insight in to impact from the rather noisy measurements, DISTORT is accurate enough.

3 A QUICK TEST

By using the DSO's persistence feature we can get a quick eyeball sense of what the TIE of the system is. The same 200 MHz BW 1 GSample/sec scope used in Clockworks AppNote001 – Jitter Spectrum measurement with a DSO is used here.

To save flipping back to that document a test case is copied here as Figure 3. It shows the edge 700 usec after trigger of the reference OCXO used; it has RMS period jitter < 3 psec and the measurement methodology calculates 12 psec RMS, which establishes the basic noise floor for measurements.[7]

[5] i.e. the peak value for frequencies in a bin is correct; if the tone is between bins then DISTORT does not attempt to calculate the true peak. This possible 3 dB variance is not a concern for the work here.
[6] Visually checking the results suggests rounding that off to 25 dB will be close enough.
[7] For those that didn't read Appnote001 the point of it was we know a US$ 50,000 setup can measure jitter < 1 psec; the question looked at there was what could be done with a middle of the road DSO costing less than US$ 1,000.

The peak to peak TIE seen in Figure 3 is higher than the baseline measured in test configuration in section 2 as the measurement interval is wider so longer term (lower frequency) jitter spectral components lead to a larger peak to peak.

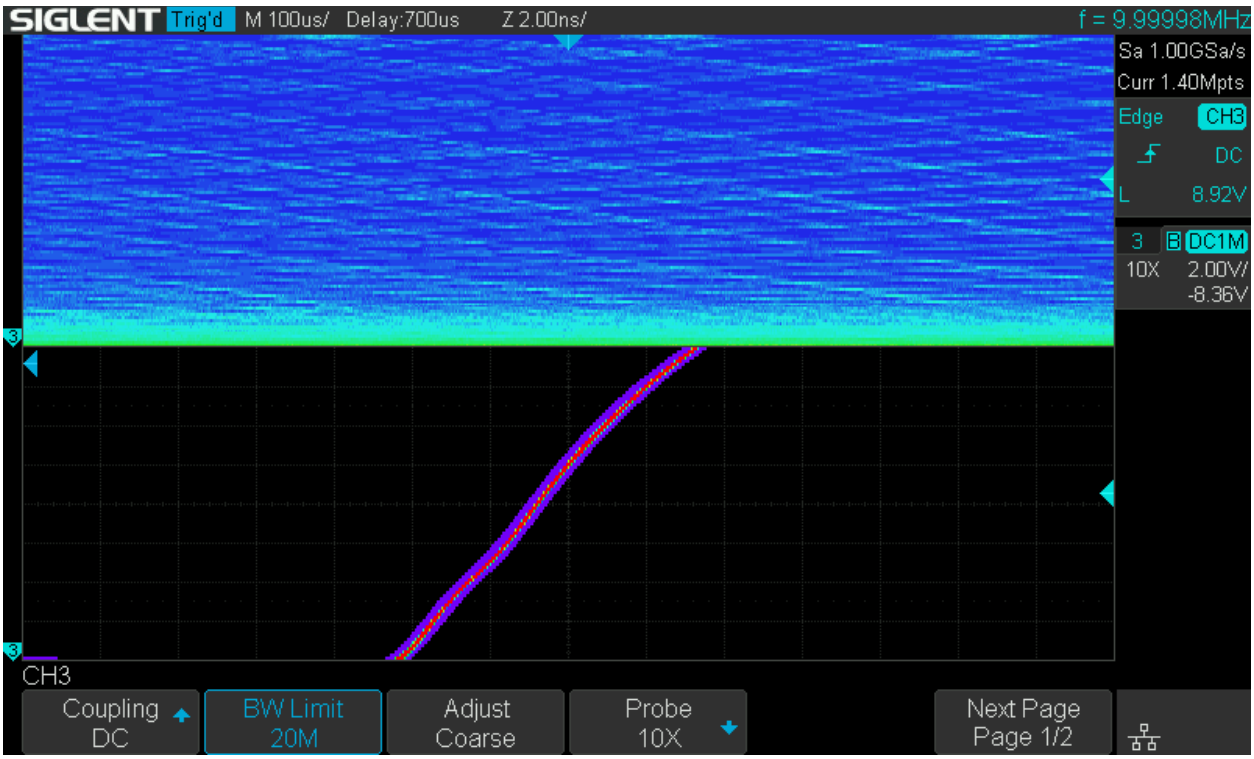

Figure 3 Residual measurement error of TIE "peak to peak" of 10 MHz test source, approx. 600 psec.

For comparison Figure 4 is the BCLK signal on the WDZ master node. We can see it traces out a slightly wider range of edge values. It's a 24.576 MHz signal vs. 10 MHz of the reference used in Figure 3. For eyeball estimate purposes we would consider this to be about as good as the reference we measured, i.e. this is the scope's combined internal timebase plus noise error at 1 msec after trigger. This works out to 300 ppb, which is not unreasonable for a general purpose DSO.[8]

[8] Looking at an edge a fixed amount of time after the trigger point is not the same as the full TIE calculation that will be performed later, but for the *order of magnitude* estimation being sought here it's more than adequate.

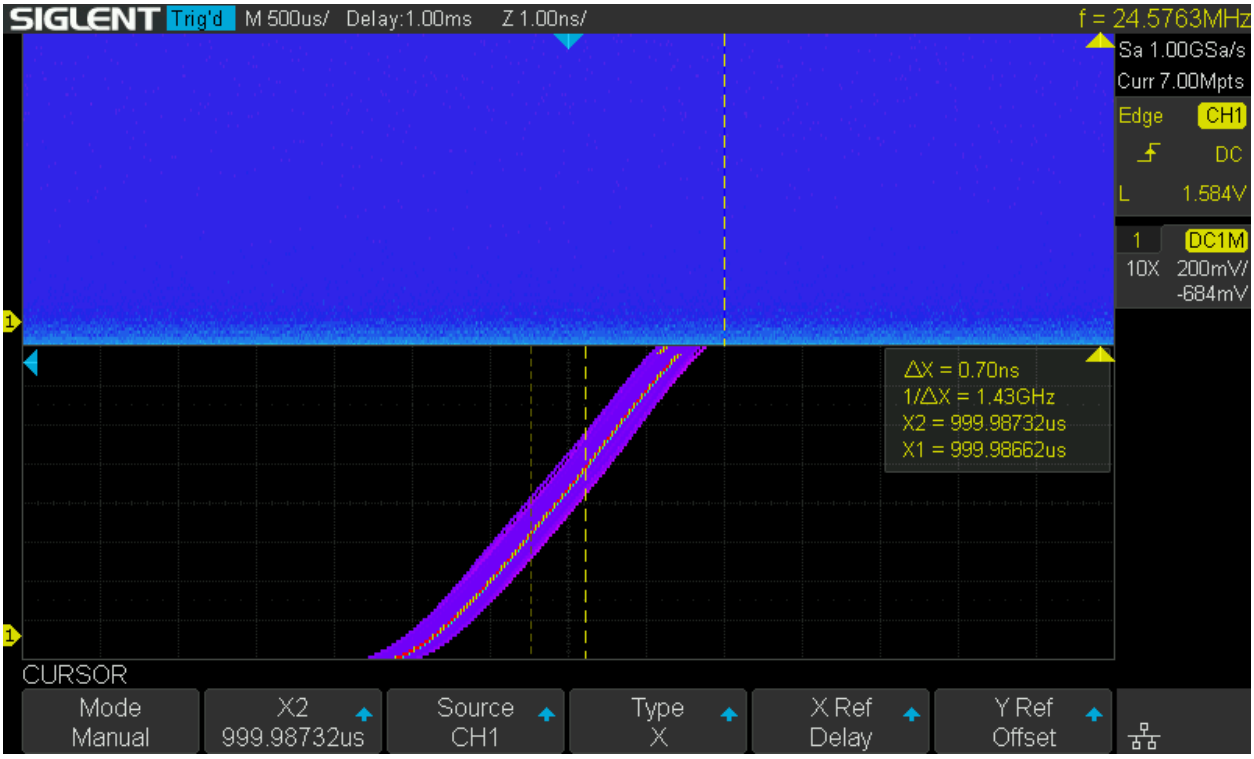

Figure 4 WDZ BCLK "peak to peak" jitter of around 700 psec; note scale is 2x the previous capture.

Figure 5 looks at BCLK on slave node 2. Ideally it would be the same as Figure 4, but instead of 700 psec peak to peak TIE about twenty times that, 14.6 nsec is measured. This is far above the measurement limits described in Section 2 and a reasonable indication that something is not right. Jitter in BCLK directly translates in to ADC and DAC sampling error, though exactly how much error and the nature of it depends on a large number of factors.

The BCLK signal comes directly from the AD2428 A²B transceiver. A reasonable check is to also look at Frame Sync (SYNC), as edge jitter should affect it in the same way. Figure 6 shows that the jitter is consistent and not a very short term variation in BCLK that evens itself out over a sample period.

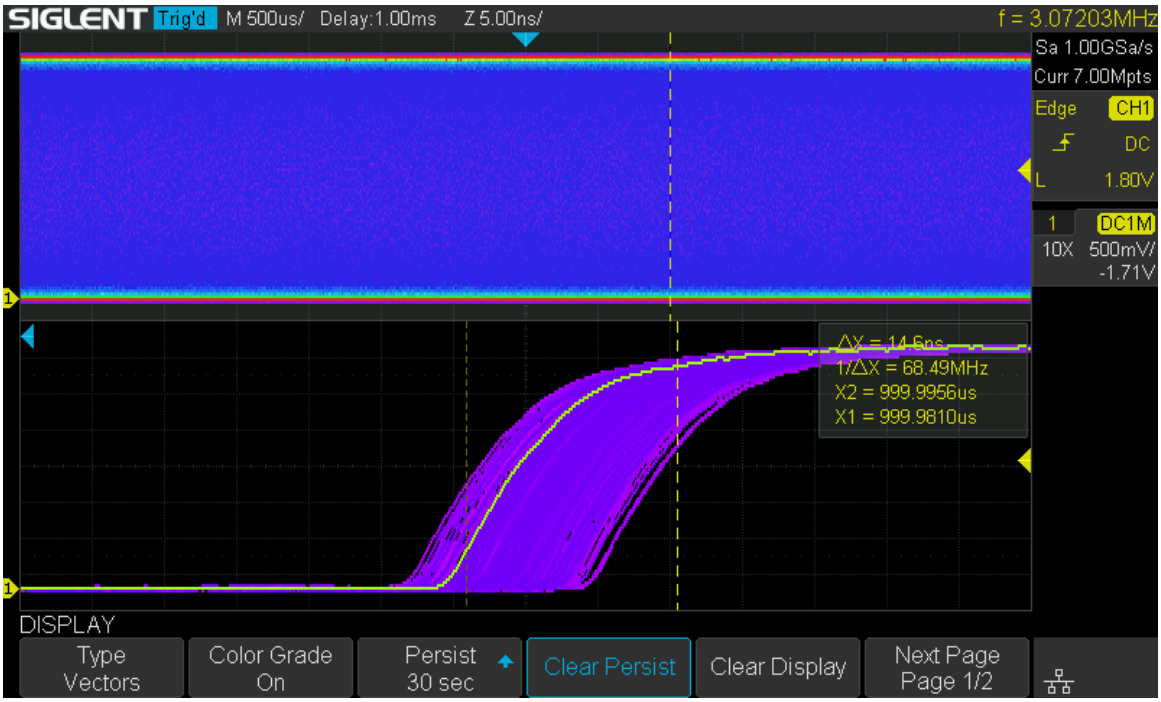

Figure 5 BCLK (3.072MHz) on slave node 2 showing peak to peak TIE at 1 msec around 14.6 nsec.

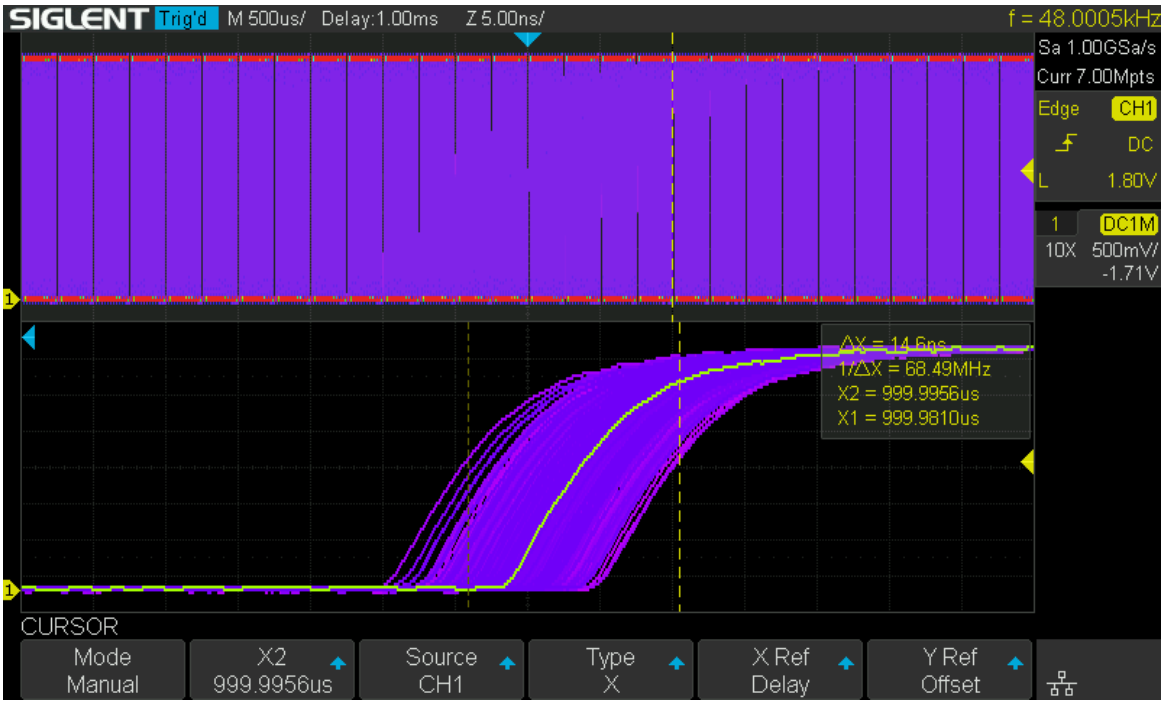

Figure 6 SYNC (48 kHz) on slave node 2 also shows the same 14.6 nsec TIE (which is expected based on the discussion in the text).

The most pessimistic assumption would be that the 14 nsec shift occurs on the alternating samples, which would translate to an abnormally large sampling error, making for a system with the performance equivalence of an 11 bit system for a 96 k sample rate.

The datasheet AD2428 RMS TIE value from Figure 2 is 1.79 nsec, so the peak to RMS ratio is about 7.8, which is in the range of reasonable factors one might expect. Though as noted earlier the TIE spectrum is of more interest than numbers like RMS and peak to peak TIE values.

The remainder of this technote looks in to details of this jitter seen by slave nodes and the implications for designing audio equipment that has specific performance goals that might range from "consumer" 16 bit 48 kHz levels to 24 bit 96/192 kHz pro-audio performance levels.

4 ADI 'WDZ BOARD BCLK SIGNAL

This board uses an ADAU1452 as the primary DSP device on the board and directly interfaces to the AD2428 A²B transceiver.

This signal is the clock input to the AD2428 master node, so jitter on this input could affect the rest of an A²B system. Jitter was not expected since it's derived from a crystal oscillator.

Measurement indicated that it was not as stable as expected. This table is created with the methodology from Clockworks Appnote001. Peak to peak TIE value is not necessarily indicative of an issue.

Across 2 msec interval (6151 edges)	**RMS**	**Peak to peak**
Cycle-cycle	120 psec	960 psec
Period (cycle – expected)	68 psec	540 psec
TIE	300 psec	780 psec

Figure 7 'WDZ board BCLK jitter measurements

Based on typical crystal oscillators RMS and peak to peak jitter for period and cycle-cycle were expected to be about 4 times less.

A histogram over the full capture of 20,000 edges doesn't show any unusual characteristics and seems to resemble an expected Gaussian shape:

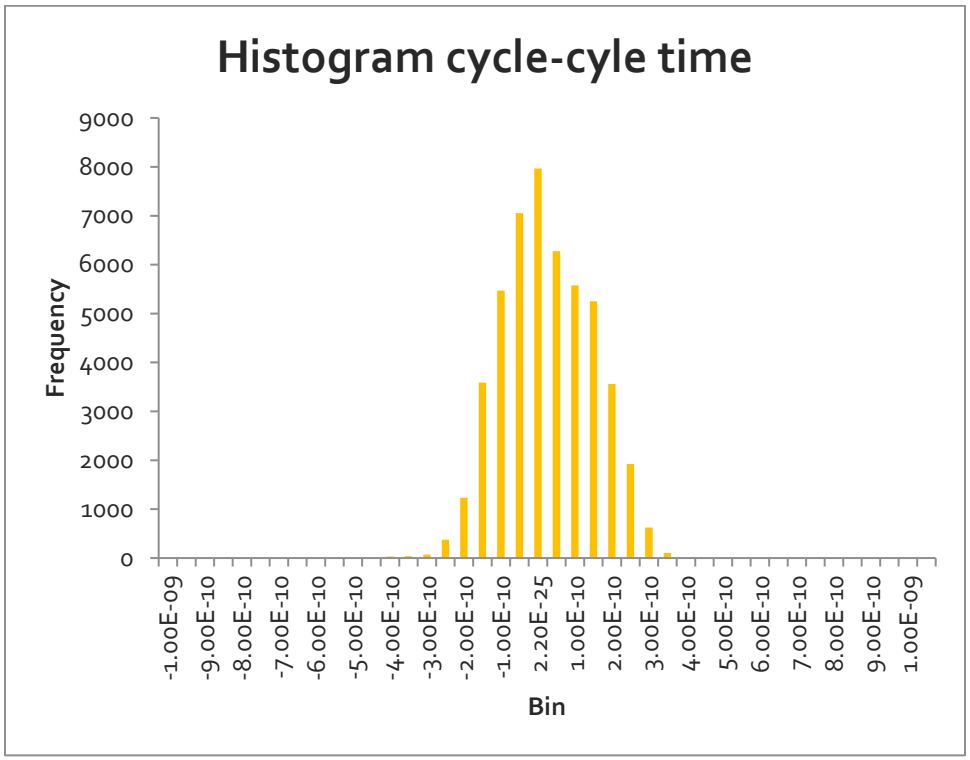

Figure 8 Histogram of cycle to cycle variation

A strong hint of a possible design issue with the board is seen looking at the TIE plot of Figure 9.

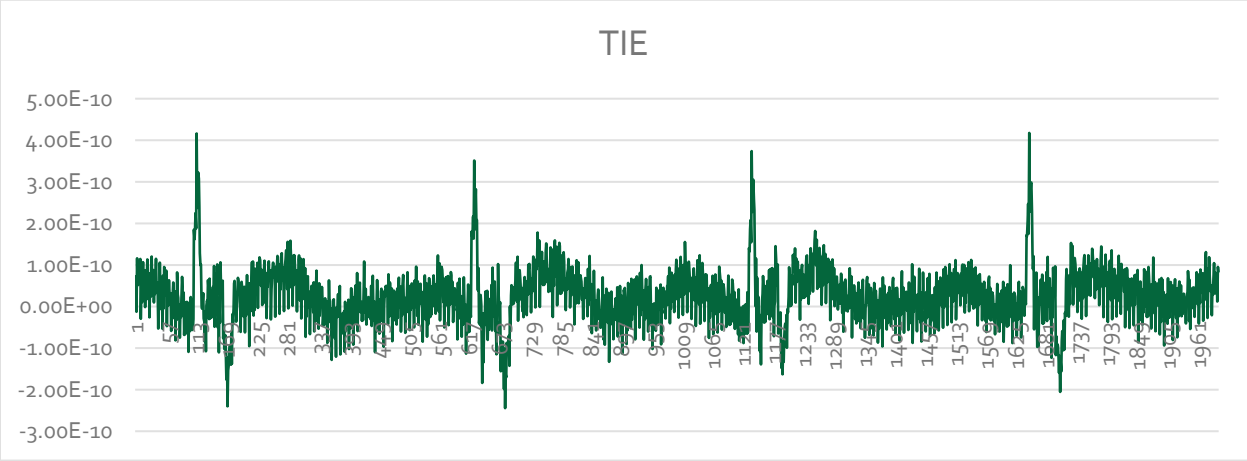

Figure 9 ADI 'WDZ EVM TIE (nsec) vs time (edge number) plot showing spike every 512 clock periods (48 kHz)

There is most likely a lot of activity on the board that starts at each sample period and that is coupling in to the oscillator circuit. There is a hint of this in the period error plot of Figure 10, but the TIE plot is much better for exposing this.

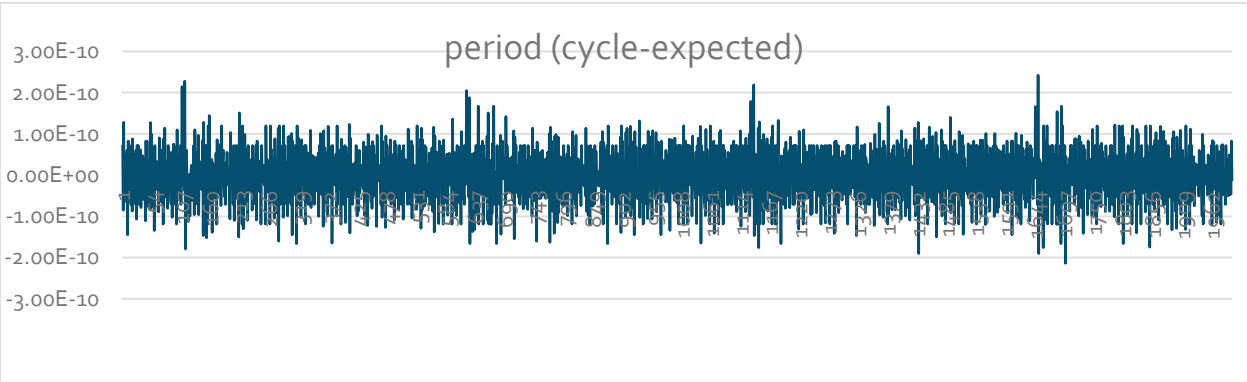

Figure 10 Period jitter shows same 512 count pattern as TIE plot

The cycle-cycle plot does not provide any additional insight. The jitter spectrum,[9] Figure 11, shows peaks at 48 kHz and multiple of that out to 384 kHz.

[9] As detailed in the app note, a Hann window is used and when there's enough data a 4K FFT is used (this is the largest one Excel supports, which limits low end resolution on larger datasets)

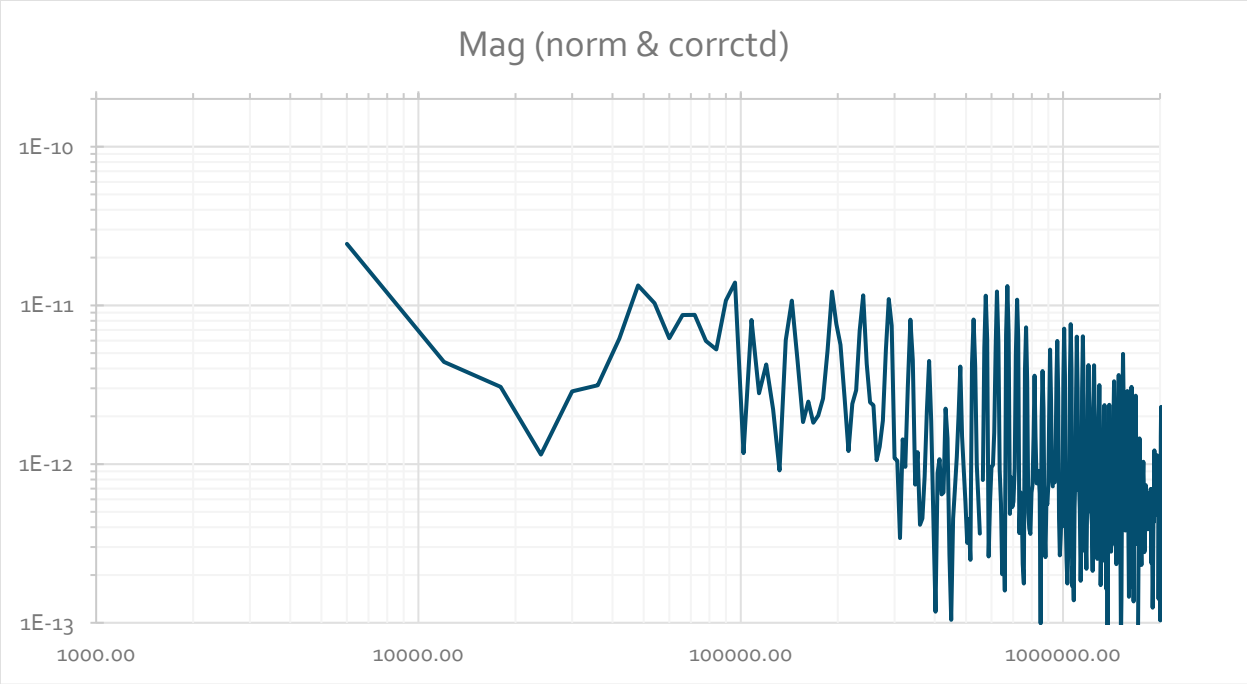

Figure 11 ADI 'WDZ EVM BCLK jitter spectrum from TIE data

The peaks clustered around 720 kHz and repeated again at higher frequencies are of unknown origin.

The AD2428 datasheet only places jitter requirements of < 1 nsec (RMS TIE) on the SYNC; BCLK is not used as the source of the PLL that creates the clock used for sending data over the A²B bus.[10]

Despite the issue observed with BCLK, which could also translate to the SYNC signal jitter, it's within the AD2428 input specifications that imply the AD2428, as a master node, can reduce the jitter to levels that allow the rest of the system to function as expected for maintaining data integrity in the SERDES clocking used for A²B.

5 SLAVE NODE JITTER

We now look at slave node jitter from two perspectives: what the datasheet defines as the expected behavior, and what we actually measure.

[10] In round numbers the PLL is multiplying the reference frequency by a factor of 1000 to create the A²B data clocks.

The datasheet does not provide any information on the jitter spectrum, though even if it did it would be difficult to determine the effect on a specific ADC or DAC.

5.1 DATA SHEET ANALYSIS

In the time frame of the original AD2410 A2B transceiver ADI wrote a short report *EE-371 AD2410 A²B Transceiver Audio Performance Testing and Results*, but did not make it available as part of the currently published documentation[11]. As the same information is contained in the RMS TIE (jitter) table (Figure 2) as well as Clockworks' own measurements, we think it's instructive to check the assumptions we've made against this second dataset.

EE-371 measured THD+N using 1 kHz versus using Clockworks proposed 11 kHz which would show a clearer impact of the jitter. As the jitter components would not be harmonic we have to assume that the ADI data just represents noise floor plus any spurs from tonal aspects to the jitter. The DISTORT calculated noise floor in the basic analysis assumes only broad band jitter, though it supports adding specific jitter tones.

The ADAU1966 that ADI uses has a typical THD+N of -98 dB (worst case -85 dB). The DR is 115.5 dB typical, implying the THD+N number is dominated by the THD, but there's no datasheet plot provided to determine if that is the case. The part has an internal PLL but no information is provided on its jitter rejection characteristics.

In the table below node 0 is the master and therefor the 1966 is being clocked directly from the hardware on that board. A number 1 dB below typical is very reasonable for actual performance of a part outside of the more idealized environment that performance for a datasheet is usually measured in.

[11] An update to this document is being worked on by Analog Devices and this document will be updated with any new information provided in that.

Node	Original EE-371 ADI measured THD+N @ 1kHz	ADI TIE RMS	DISTORT simulated noise floor from random jitter's effect on 1KHz sine
0 (master)	-97 dB	-	-
1	-94.5	1.57 nsec	-111 dB
2	-93	1.79	-110
3	-92	1.91	-109
4	-90.5	2.04	-108
5	-89.5	2.15	-107.5
6	-88.5	2.27	-107
7	-87	2.44	-106

Figure 12 ADI EE-371 (2016) measured THD+N for ADAU1966 DAC (col. 1), RMS TIE, and theoretical DR (noise floor).

Even with the largest jitter values the additive noise would increase the total noise by about 1 dB (i.e. -98 dB + -106 dB = -97 dB). The assumption about the jitter being random may be wrong.

The change in the noise floor from the increasing jitter between nodes 1 and 7 is 5 dB in the simulated data but almost 10 dB in the measurements by ADI.

There are two mysteries present here; higher than expected noise values, and they grow faster than expected.

If the ADI measurement was for DR (Dynamic Range) on a DAC that would perform around 115 dB (which the 1966 does) then the performance numbers would be dominated by the noise from random jitter *if* the DAC did not reduce it (which we assume it does by some unknown amount).

5.1.1 EE-371 REVISION ADVANCE INFORMATION

As part of ADI's ongoing update the measurements of EE-371 performed on the AD2410 have been performed again using AD2428 based nodes with the ADAU1966 DAC, which lists THD+N as -98 dB. Degradation in THD+N between node 0 and 7 is reported as around 3 dB.

This is a very positive outcome and does fall in line with the theoretical aspects of Figure 12's third column. It also would imply that the AD2428's jitter characteristics are such that both voice and low end consumer applications with 'reasonable' DACs will meet performance goals without additional clocking consideration.

A different, older unpublished ADI study using the higher performance AD1955 (-110 dB THD+N) shows that performance could potentially drop by 12 dB in the presence of the AD2428's TIE.

5.2 MEASUREMENT OF BCLK ON SLAVE NODE #2

Using the most accurate section of the captured data from the 'scope to keep the jitter measurement noise (< 20 psec RMS) low the following is measured. The datasheet for the AD2428 doesn't directly specify BCLK jitter for I²S, though table 4 defines tBCLKOJ for PDM modes and there's no obvious reason why this wouldn't be the same clock as I²S mode; the datasheet specifies the worst case cycle to cycle jitter as 175 psec, and the measurement noise in the setup used contributes some as well here. The worst case RMS TIE values is 2.6 nsec; for those two numbers the measured results of Figure 13 shows the AD2428 is operating within specifications.

Across 2msec interval (6151 edges)	**BCLK RMS**	**BCLK peak to peak**
Cycle-cycle	170 psec	1.3 nsec
Period (cycle – expected)	180 psec	1.4 nsec
TIE	2.1 nsec	10 nsec

Figure 13 Slave node 2 BLCK jitter measurements

The statistics of the above table do not change by any appreciable amount when measured across the full dataset of captured edges (20,000 measurements). The one exception is peak to peak TIE rises to 17 nsec, but that is expected due to the longer period variations in TIE. Though longer period here means +/-3.5 msec relative to the trigger, the jitter component frequencies that cause the increased peak to peak measurement are probably on the order of a few hundred Hz.

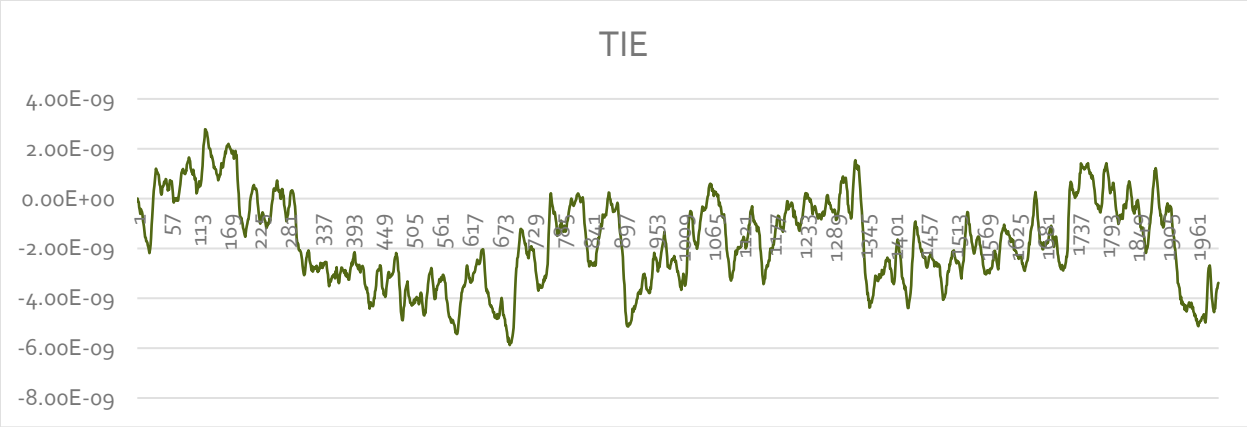

Figure 14 Measured TIE vs. edge number for BCLK (3.072 MHz) on node 2 across 2000 edges. Unlike BCLK on the 'WDZ board, there's no obvious match to the frame rate. OTOH it is not a slow smooth variation, in places we can see it jumping a few nanoseconds across a few sample times. (Time axis is in seconds)

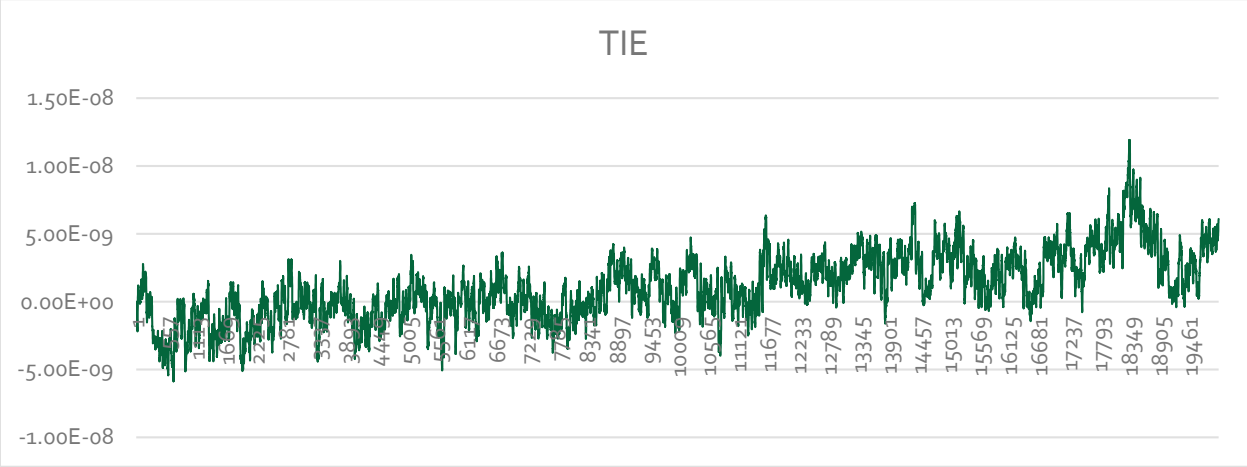

Figure 15 TIE vs. edge number for node 2 BCLK across the full 20,000 sample dataset (6.5 msec). We can see the longer period variations, as well as how this results in the 14.6 nsec peak to peak measurement on the scope.

Figure 14 and Figure 15, based on visual inspection, might seem to show some sort of underlying timing pattern. Figure 16, the jitter spectrum, shows a strong peak at 6 kHz (1/8 the sample rate) and 12 kHz (1/4 the sample rate), as well as 96 kHz, but no strong peak at 48 kHz that might be associated with the basic system timing. The peaks at 21750 Hz and 26250 Hz don't

seem to have a logical connection to the data rates, though the FFT bin size is 750 Hz and therefor there's a wider range of possible frequency ratios that could offer an explanation.

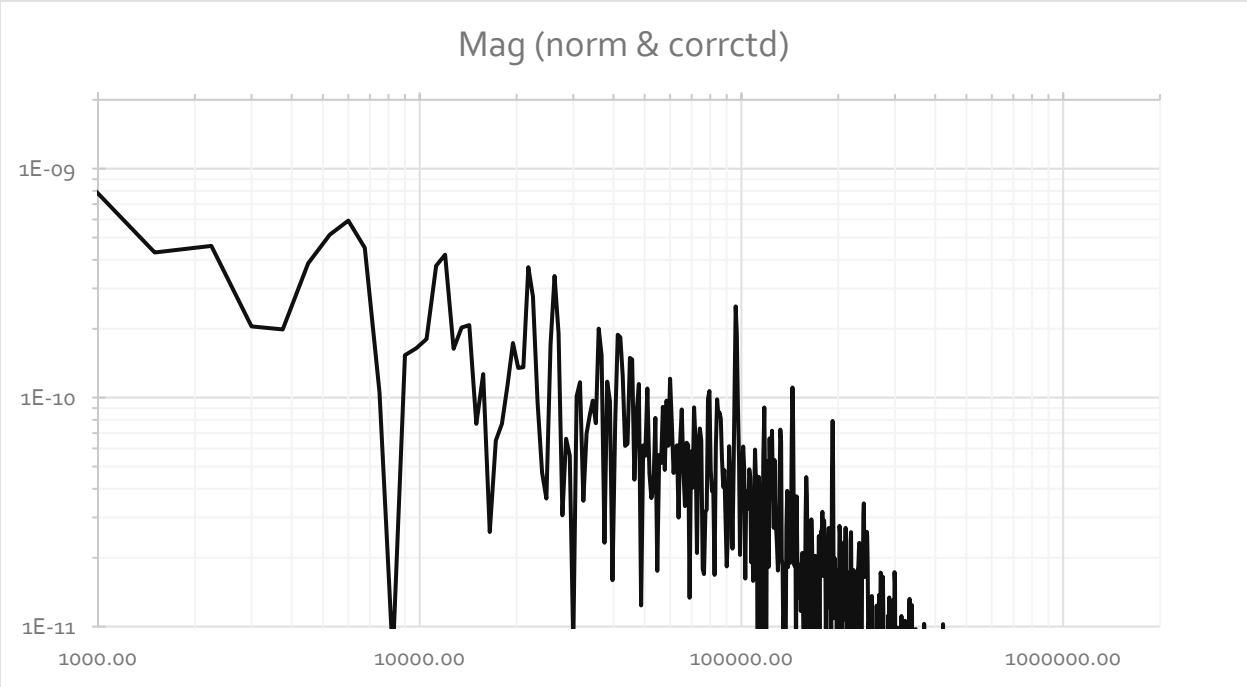

Figure 16 BCLK TIE spectrum. While a few peaks appear a longer FFT and several averages of them would be needed to create a more in depth understanding. (4K point FFT, Hann window)

Looking at SYNC provides slightly more resolution at the lower frequencies than the BCLK TIE spectrum. Since Frame Sync is derived from BLCK its edges would be expected to match the same jitter as BCLK. As we're measuring over 64 BCLK edges and we see how the BCLK TIE can all head in one direction, we might expect the SYNC period jitter is higher than BCLK, and indeed it is.

Across 7 msec interval (333 edges)	**SYNC RMS**	**SYNC Peak to peak**
Cycle-cycle	3.4 nsec	22 nsec
Period (cycle – expected)	2.0 nsec	14 nsec
TIE	2.6 nsec	14 nsec

Figure 17 SYNC measured jitter values on node 2.

As we might expect the statistics for TIE do not change much, but the period related jitter numbers do become significant.

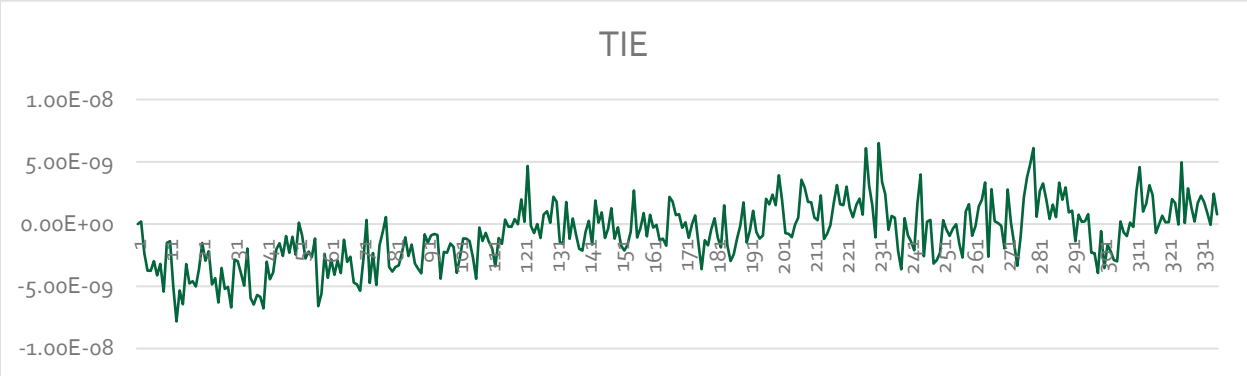

Figure 18 (Frame) SYNC TIE across the measurement time window (7 msec).

Figure 19 calculates the spectrum, though the limited data means only a 256 point FFT can be used so again not a lot of resolution at the lower frequencies. The three lower frequency peaks appear to be 672 Hz (shown later) and harmonics of that, though this is not a sub multiple of 48 kHz.

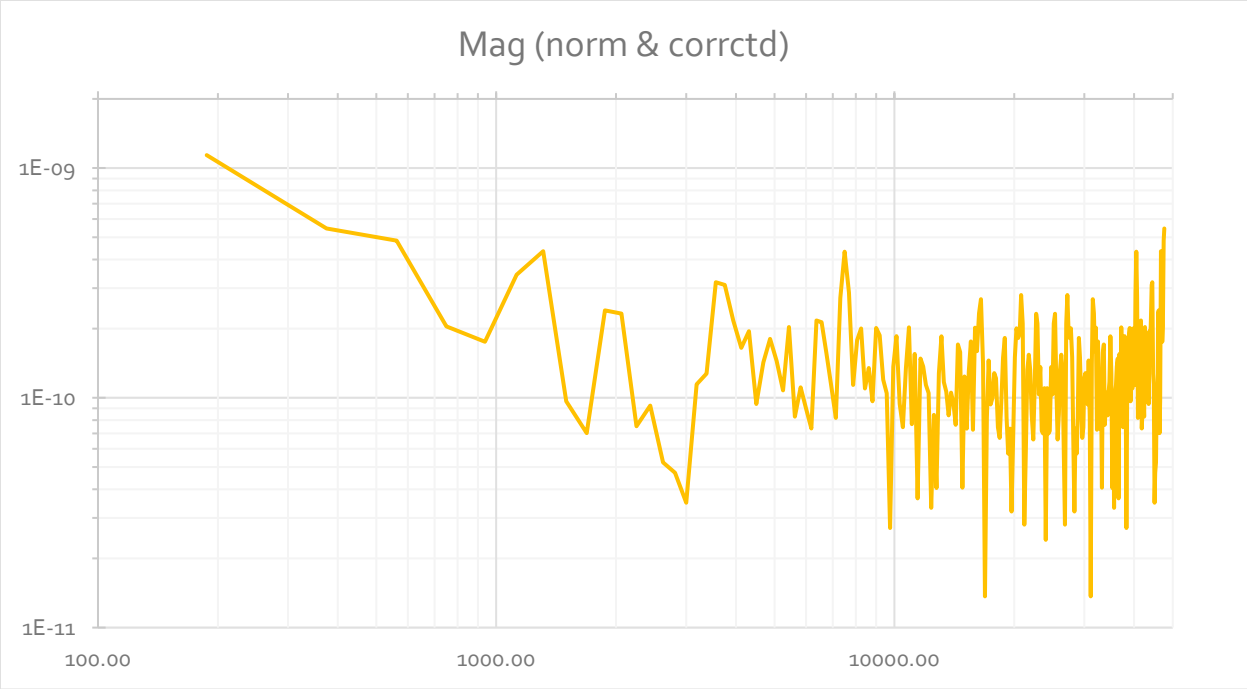

Figure 19 Frame Sync TIE spectrum (256 pt FFT, Hann window)

The direct jitter measurements of BCLK can also be compared with spectrum of the clock signal using the DSO's spectral computation feature, Figure 20. The wide spreading around the fundamental is probably from low levels of random jitter that the jitter spectrum shows rising with decreasing frequency. The larger spikes around the center are spaced at multiples of 48 kHz.

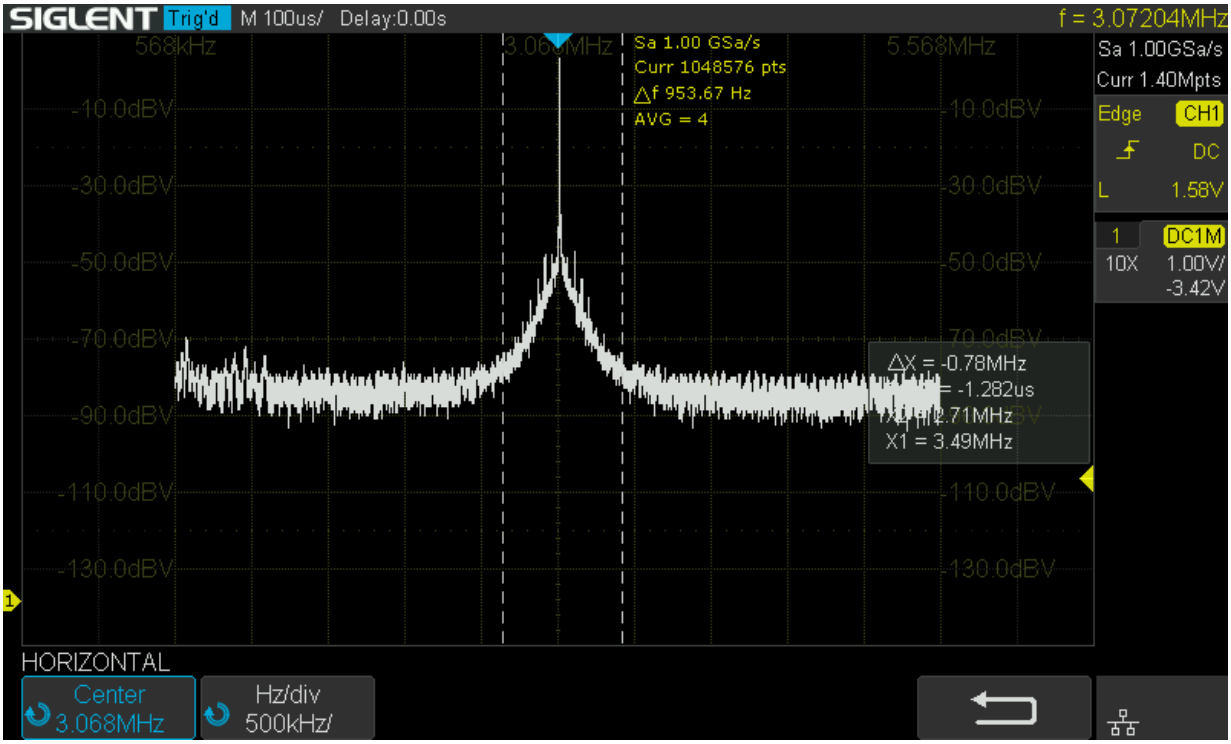

Figure 20 BCLK on node 2 spectrum

Figure 21 shows a zoomed in view and we can see the 12 kHz sidebands from the jitter components identified in Figure 16.

We can also examine the Frame Sync signal spectrum as captured in Figure 22. We can see the largest peak there and its harmonics would match with the lower peaks in the jitter spectrum in Figure 19.

Despite the places where the jitter components and clock sidebands match up, there are plenty of non-matches as well as uncertainty over the cause when the frequencies don't seem to have a connection to the sample rate. Same may instead be related to the A²B bus 49.152 MHz bit rate, but as all of this is internal to the ADI parts there's not a lot a designer can do to clean up the I²S clocks without additional circuitry.

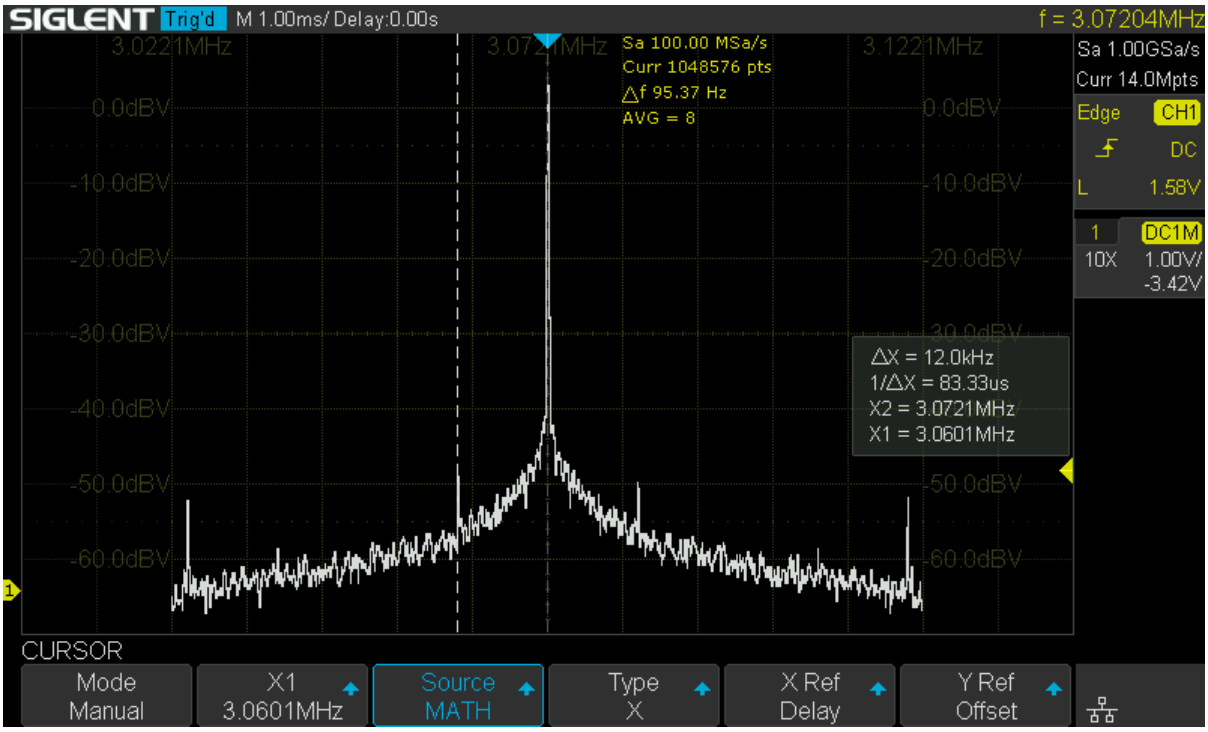

Figure 21 BCLK spectrum close in showing 12 kHz jitter component

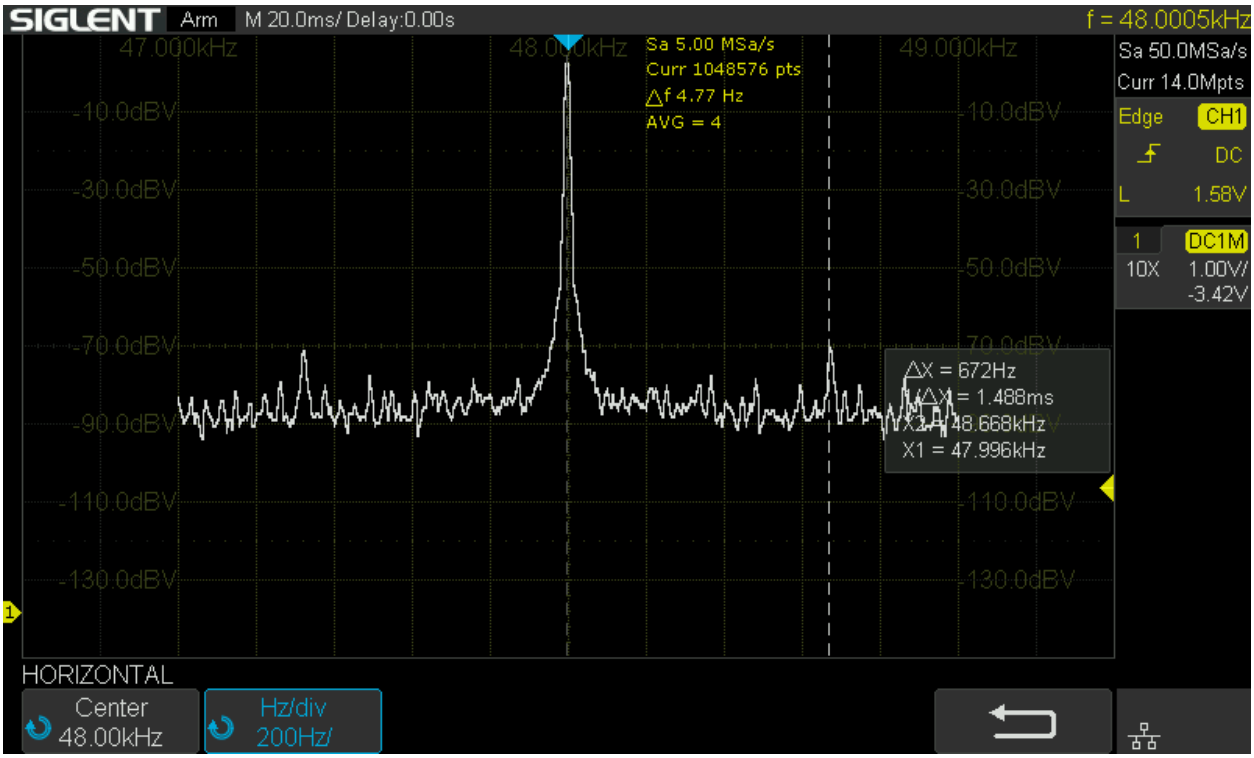

Figure 22 SYNC spectrum look at close in frequencies.

5.2.1 NEXT

There are a couple of paths to move forward from this initial data. Capturing statistically larger amount of data (and with less measurement noise) would allow separation of the jitter in to the deterministic and random portions, which could provide more insight as to the cause(s).

This does not help determine how a specific ADC or DAC will perform when fed the jittery clock. Even with full statistics and very accurate models of the parts it would still need to be verified on the actual hardware. At best the results here establish an upper bound for problems.

The point here is to provide enough information about the jitter from the AD2428 clock outputs so that the designer knows what to expect, and to ensure that systems are fully characterized prior to a final design.

Applications where the final system is like an internally amplified speaker that has no direct measurable electrical output can hide a lot of sins when measured by what comes out the driver. OTOH a professional audio ADC or DAC will receive thumbs down from reviewers with even a hint of questionable results.

5.3 SYNTHESIZING THE OUTPUT BASED ON JITTER

Since we have a jitter spectrum we can use the DISTORT software to make an approximation to what the output would look like through a DAC with no clock cleanup and very low internal noise.

Figure 23 shows the possible output spectrum when using the SYNC spectrum and RMS numbers as the parameters used by the DISTORT program. Take it with a grain of salt as the assumptions used may not be totally valid. The -100 dBFS side lobes, while not audible, would probably be questioned by a reviewer. The close in -93 dB tones would likewise call attention to themselves unless the analysis had low FFT resolution, which is not likely.

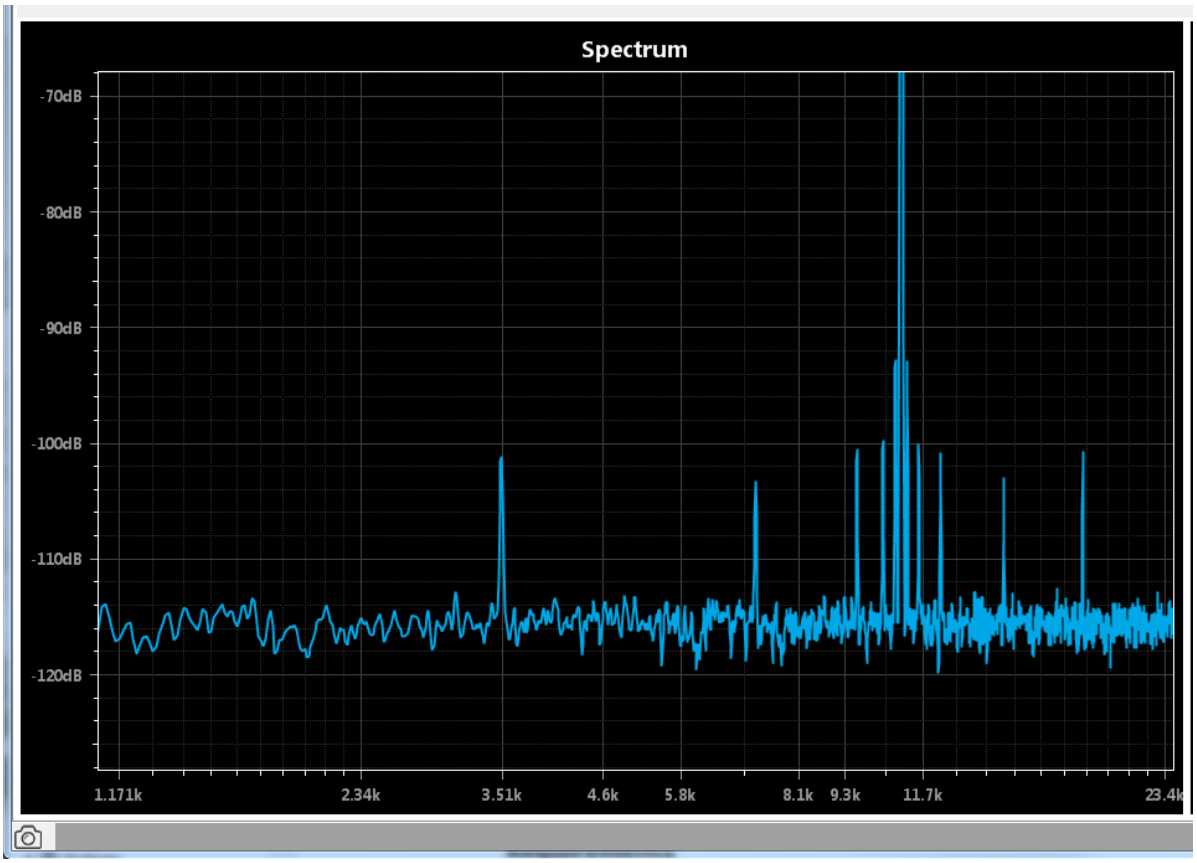

Figure 23 Expected spectrum of -1 dBFS 11 kHz based on measured Frame Sync jitter spectrum. 4096 pt FFT (BH-7 window), which means the noise floor from jitter is -95 dBFS in this case. Approximated here is that 1.5 nsec RMS of the noise is random and the rest is from specific jitter frequencies; this approximation may not be valid.

Figure 16 uses the BCLK spectrum under a similar set of assumptions. As the FFT frequency resolution is more granular the locations of the sidebands will be different. Also the random jitter is assumed to be lower as it's spread across more clock sample periods than the Frame Sync case.

Neither Figure 23 nor Figure 24 are necessarily the specific pictures we would expect as the DAC is an unknown, as well as our jitter spectral data to feed in to the DISTORT program is limited. Despite these shortcomings it does help give a feel to what might happen in a real system.

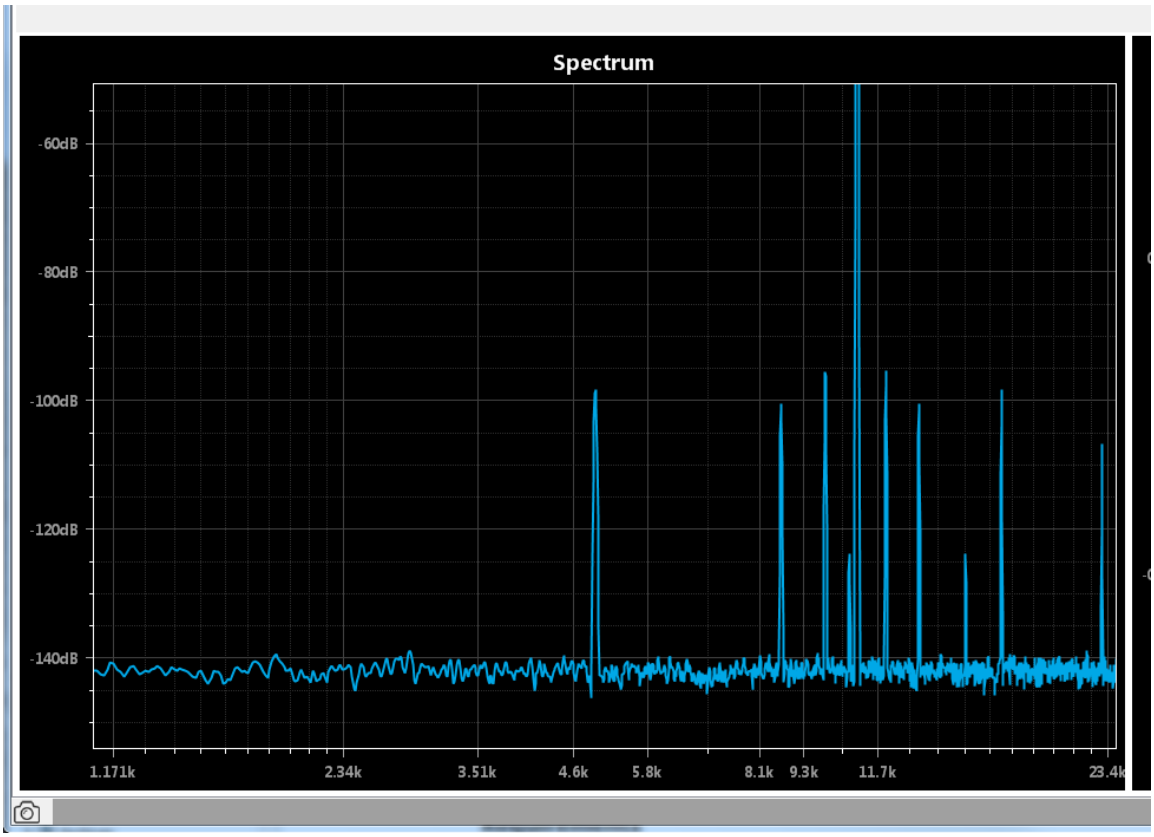

Figure 24 Figure 15 Expected spectrum of -1 dBFS 11 kHz based on measured BCLK jitter spectrum. 4096 pt FFT (BH-7 window), which means the noise floor from jitter is -115 dBFS in this case. Jitter below 1 kHz is not accounted for due to limited FFT resolution of the measurement.

6 REAL LIFE

Node 2 in the test setup uses an ADAU1761 as a DAC. It has an unweighted SNR and DR of 98 dB (typ) and THD+N of -92 dB. It's 0 dBFS output voltage is -6.7 dBV in the single ended configuration used on this board. It has an internal PLL so the expectation is that the input clock jitter will not directly translate to the output. However its lower end characteristics for DR performance will mask problems that would be visible in parts operating with DR closer to 110 or 115 dB.

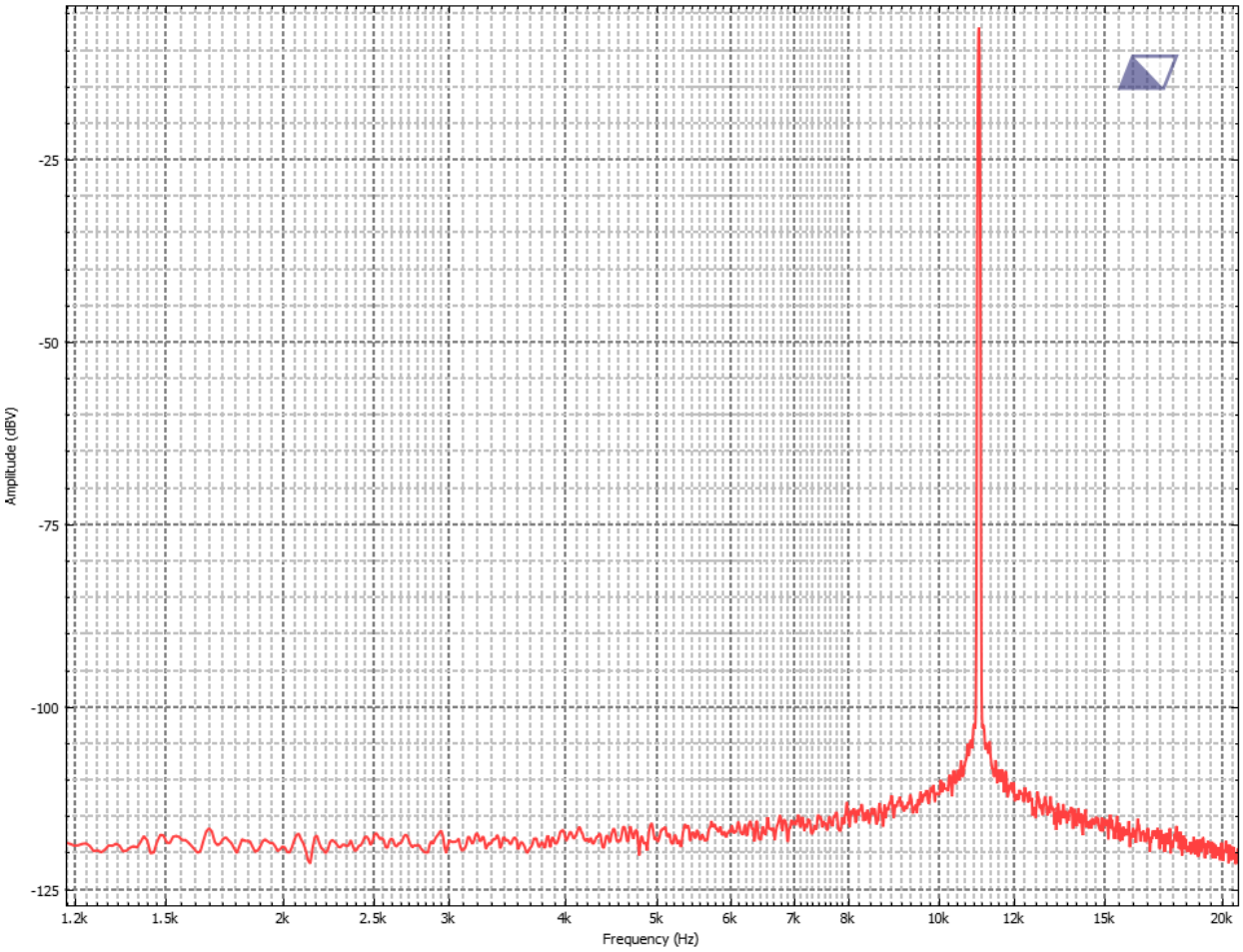

Figure 25 ADAU1761 output with 11 kHz input (4K FFT 32 avg)

From the analog output captured in Figure 25 we don't see any indication of the spurs expected from the jittery I²S clock. There is some low level broadening of the 11 kHz tone, probably from the higher levels of random low frequency jitter. If the ADAU1761's PLL is filtering the jitter this plot would back that claim.

Comparing with a 1 kHz tone in Figure 26 the spectral FFT noise floor with the 1 kHz tone ranged from 5 to 10 dB lower, which is expected if random jitter was occurring.[12] We can use DISTORT to estimate the spectrum with just random jitter from a flat and 1/f (close-in) spectrum (Figure 27) and get a general set of characteristics that match what we measure.

[12] To determine the actual noise floor in dB the plot has to be integrated and corrected for the FFT used, but we can eyeball it here to say a 1 kHz test tone raises the noise floor less than a 11 kHz one.

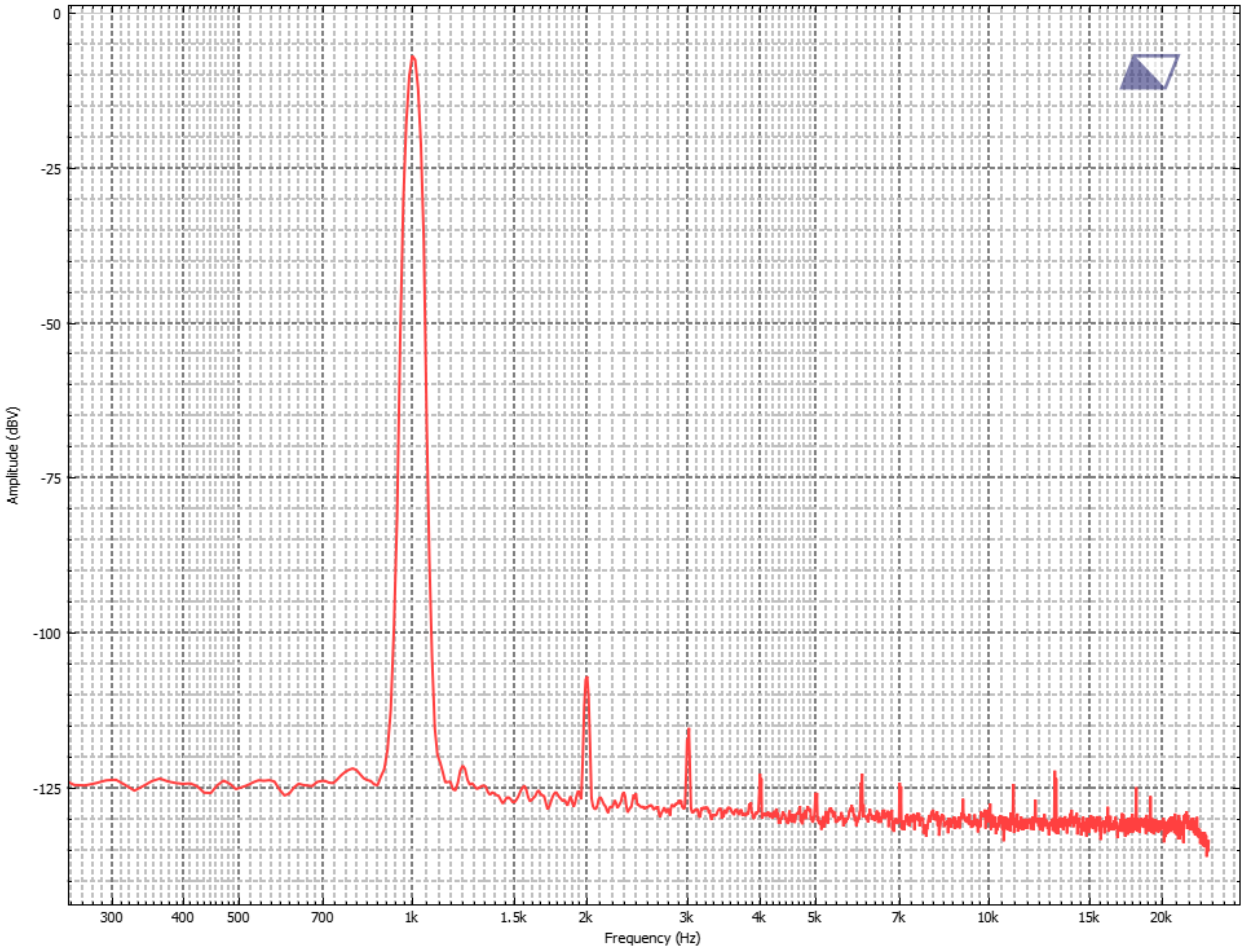

Figure 26 ADAU1761 1 kHz tone (4K FFT, 32 avg)

The same settings that create Figure 27 also create a spectrum for a 1 KHz tone, that when added to the ADAU1761 noise floor, would produce a shape to the floor like that shown in Figure 26.

This test, despite using a DAC with limited DR, suggests that the A²B jitter has degraded the noise floor even though we didn't consider that the clock jitter is also capable of shifting the modulator's shaped noise back in to the audio band; the DISTORT simulation is only considering noise due to the idealized sampling of the analog waveform.

As previously elaborated, the specifics of the ADC and DAC design (clocking, modulator, etc.) will all combine to in ways that are very complex to predict in the presence of clock jitter. Measurement under a set of conditions to expose problems is considered as the most practical way to tease out these subtle behavioral aspects.

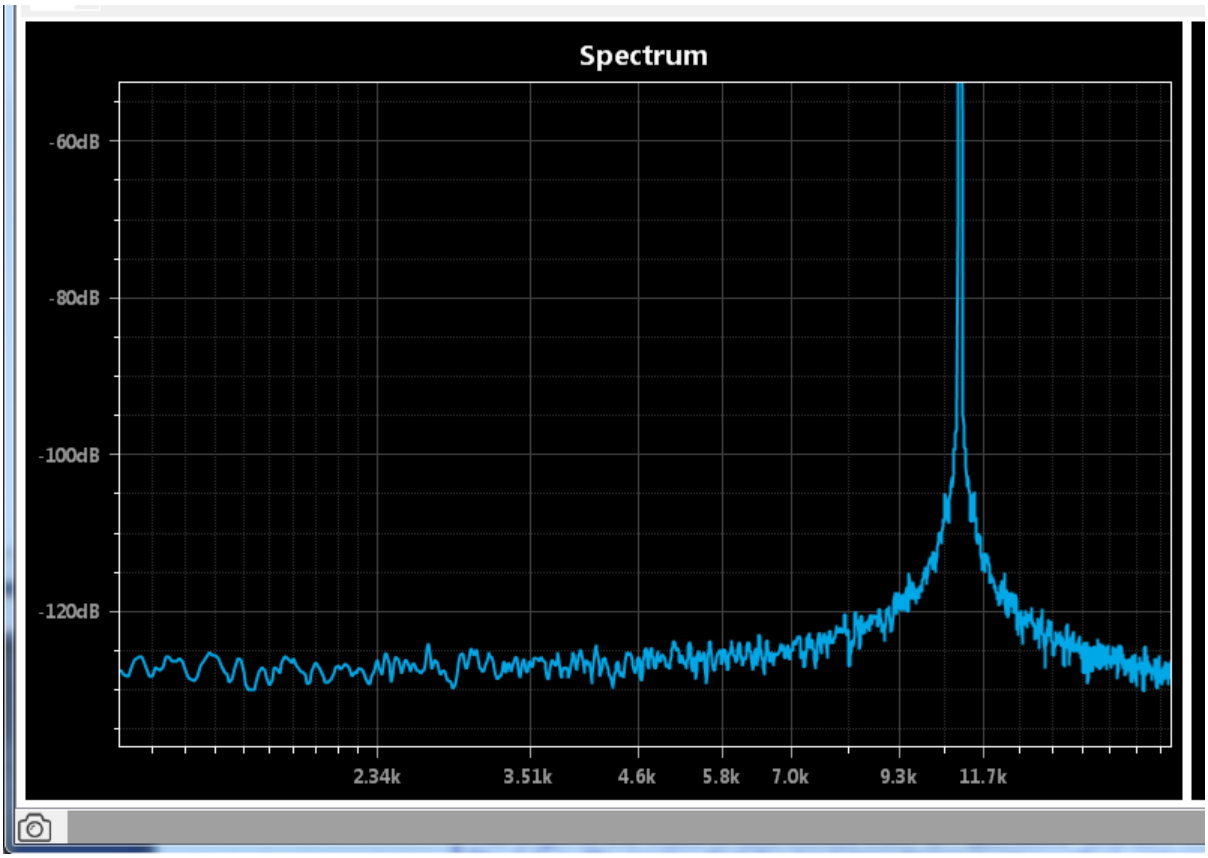

Figure 27 DISTORT simulated jitter with 11 kHz tone, 400psec random, 2 nsec close in jitter (4K FFT, BH-7 window)

7 WHAT TO DO?

This TechNote only looked at a short 2 node chain; the AD2428 datasheet shows the worst case jitter at the last A²B node could be almost 3 times greater than what was determined here.

Designers of high performance systems, unless the chosen ADC and DACs have very aggressive clock cleanup internally, will want to include a clock clean up chip in their hardware designs. Cirrus 2200/2300 parts have long been used for that purpose. ASRCs would probably be an expensive overkill, as well as add latency to what currently is a very low latency system (2 samples).

8 SUMMARY

The levels of I²S TIE (jitter) specified on the AD2428 datasheet require that all audio designs consider if it may impact the hardware's performance relative to the design goals. These parts' TIE (Time Interval Error), which is the primary concern for ADC and DAC designs, and the uncertainties of how ADCs and DACs performance varies with TIE, creates the need for testing of proposed ADC and DAC hardware. With an observed peak to peak TIE value in the 15 nsec range and a set of worst case assumptions system performance could fall to that of 12 bit converter.

The jitter values associated with the AD2428 are large enough to allow the use of middle of the road DSOs (see the reference to Clockworks AppNote001) to analyze and determine possible sources of problems for all but the most high performance audio/signal processing applications.

As Clockworks tests more of the ADC and DAC hardware options that started this investigation new TechNotes will be published that could help guide system designers in decisions related to clock jitter in high performance audio applications. In the meantime this TechNote can be used to guide those investigations.