TECHNOTE 011

A²B PERFORMANCE WITH A CUSTOM BUS POWER SCHEME

Rev 1b

27-Jun-24

Signal Processing

http://clk.works/

1. TABLE OF CONTENTS

In addition to off the shelf development boards Clockworks' custom design work sometimes includes A^2B hardware where the bus power scheme has requirements that are not addressed by ADI's newer CFG4 (24V, 50W) power schemes.

In this example we look at the analysis and measurements for a custom bus power scheme where the requirements for a custom subordinate nodes (we'll call it type C) were as follows. Other types of subnodes would exist that would require bus power (type B) and others that could provide 24V at 2amps of bus powered (type L).

- C (custom) nodes would need to be galvanically isolated from the A^2B bus
- C nodes would be locally powered
- C nodes would not be able to supply bus power
- C nodes need to detect bus power is present so they can power up and execute the A^2B discovery protocol.
- Connectors and cables would be 2 wires, i.e. A^2B data and bus power must be transported on the same wire pair.
- Type B (bus powered) nodes would need no more than "a few" watts of power.
- The root/main node would be able to supply 24V at 2A of bus power.
- The connection order of sub nodes (types C, B and L) could be arbitrary, and B and L nodes may or may not be present in a given system.
- AD2437 device is to be used to support longer cable lengths and CFG4 power.

Though not planned for deployment, a system might have up to 16 C nodes, though the full complement would preclude the other node types. A more common configuration might be 4 C nodes, and 4 B nodes, along with the root/main node.

1 INTRODUCTION

ADI's reference platforms do not include systems where galvanic isolation is a requirement.

Galvanic isolation is easily obtained using transformers designed for Ethernet. As an example Clockworks offers a line of modules for galvanic isolation to be added to any A2B system; in the example of Figure 1 the module also includes isolated DC-DC power conversion to support downstream bus power.

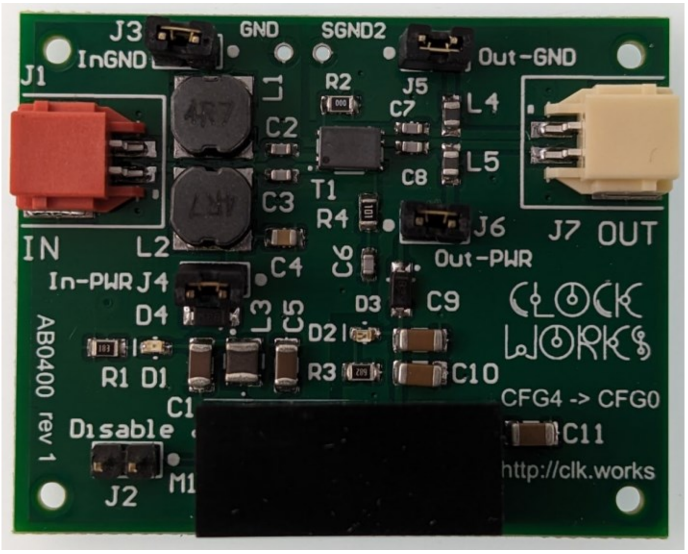

Figure 1 Clockworks A^2B galvanic isolation module

A^2B uses Manchester encoding so there's no appreciable data signal in the decade below the primary bus frequency, which we'll use 50 MHz as a reasonable approximation. As pointed out in Clockworks TN007 document, the A^2B bus is not always active, so there are low frequency components related to the 48 kHz frame rate of the bus. However they do not convey data and we can ignore them.

Given that a system might be connected in an order like this:

Root/main → C → C → C → B → C → B

We need a way to get the power from the root/main node to the last B node, and we're constrained by only having 2 wires.

This document explores things that were looked at in determining that the custom scheme would be reliable. As with anything engineering, there was a pragmatic choice of what to test and what to skip over; mostly informed by prior work.

2 SUMMARY

After considering a few ideas it was felt that the simplest solution would be to have each of the C nodes pass bus power to the next node. Furthermore the bus power scheme would follow ADI's recommendation for 2 wire bus power with the CFG4 power scheme. This allows the root/main node and the B (bus powered) and L (local powered) sub nodes to use ADI's design recommendations to support line/fault diagnostics for the B and L node types.

To do this the C type nodes simply pass "DC" from the A²B transceiver's A side (upstream) to the B side (downstream), though in real life there's nothing stopping power from being sent up the bus. That's probably a bad idea though.

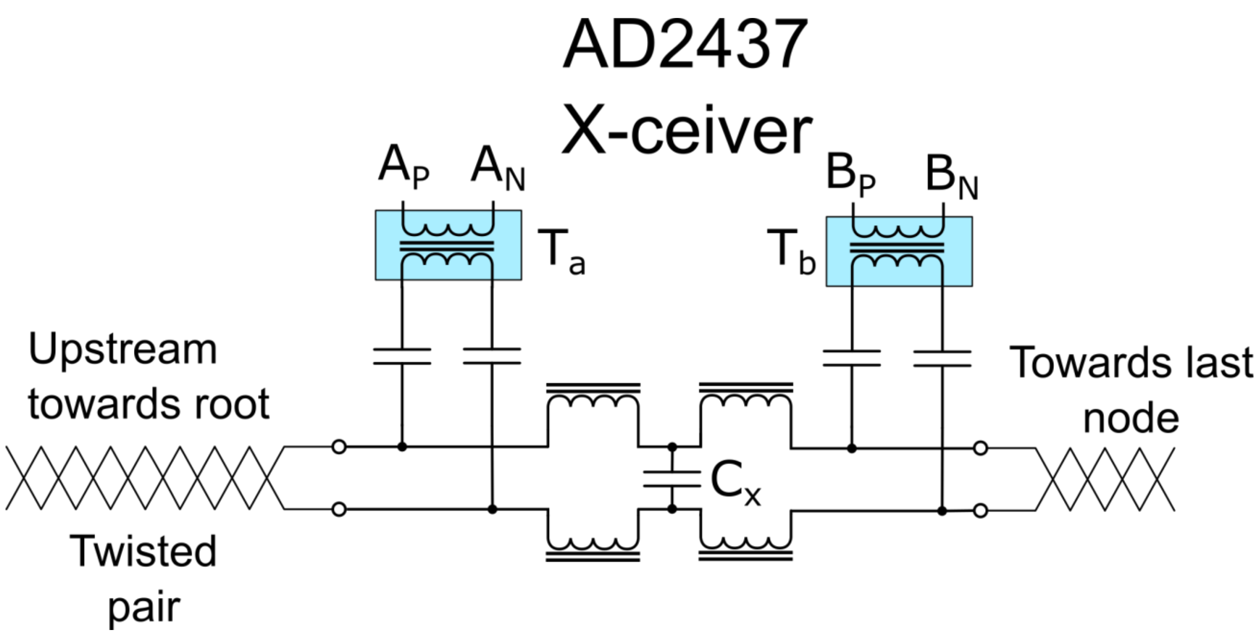

Figure 2 Custom 2 wire power scheme for custom node (type C in the example).

In Figure 2 we present a simplified view of the bus power scheme. Transformers Ta and Tb provide galvanic isolation. The actual schematic is shown in Section 5.

The four inductors block the A²B data but pass DC. They must attenuate the A²B data enough to prevent crosstalk between the A and B ports of the AD2437. We need to sense that bus power is present; we can do that by placing an optoisolator in parallel with Cx in Figure 2 to provide a galvanically isolated control signal to turn on the power.

The inductors used, Bourn SRN6045-4R7Y, have a maximum impedance at 44 MHz (Figure 3), after which it decreases with rising frequency due to the parasitic capacitances. The LTSpice model for the Bourns inductor is a little more optimistic about the high frequency reactance (Figure 4).

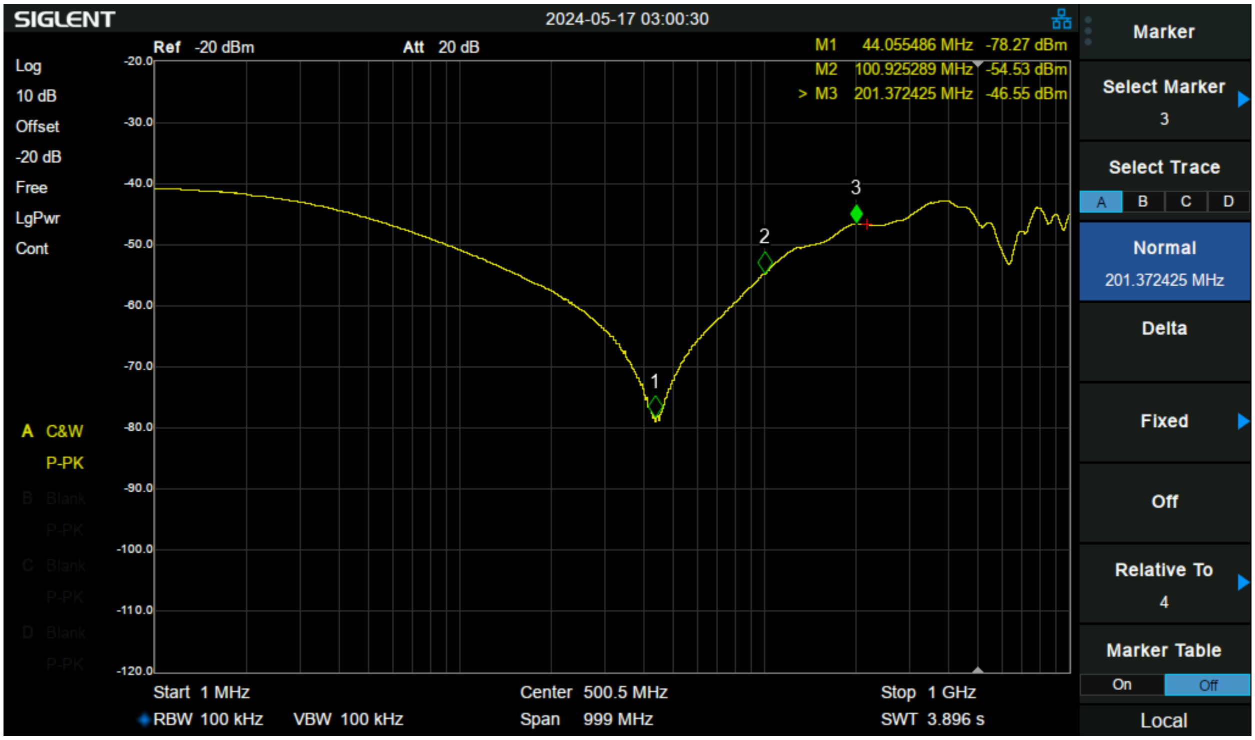

Figure 3 Measured response of SRN6045 4.7uH inductor.

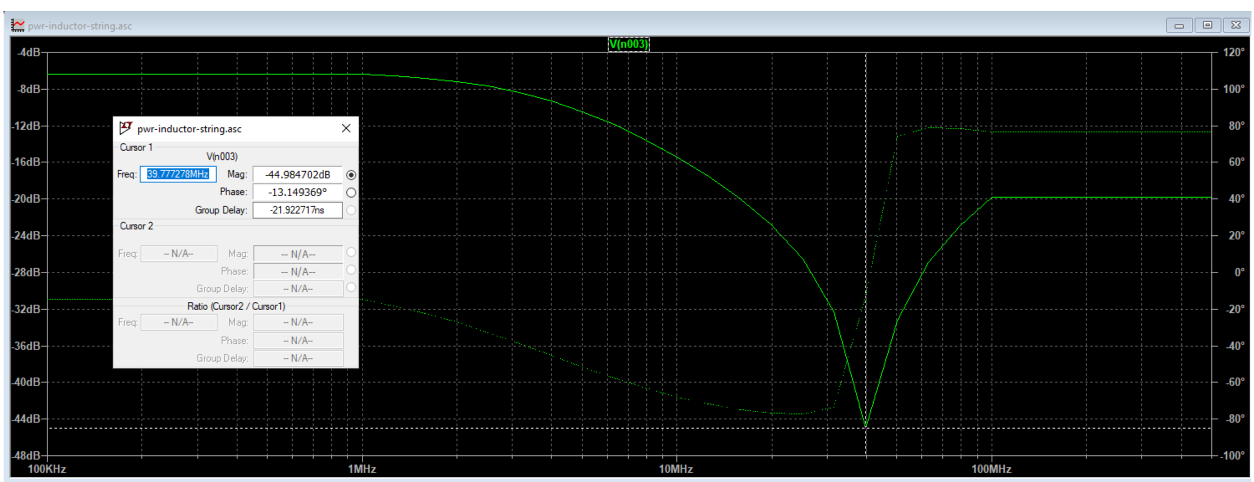

Figure 4 LTSpice results for the inductor.

One concern was the lower impedance at high frequencies would appear as a load on the A^2B signaling to the point where it degraded signal level.

2.1 TRANSFORMER

Another question was the impact of the transformer (Wurth 74930000) that was used for isolation.

Wurth makes a LTSpice model available and it shows a pretty deep loss around 158 MHz, which as the 3rd harmonic of the primary frequency is probably something that we would want to be careful about attenuating. Figure 5 is equivalent to the fixturing used to measure the transformer with the spectrum analyzer.

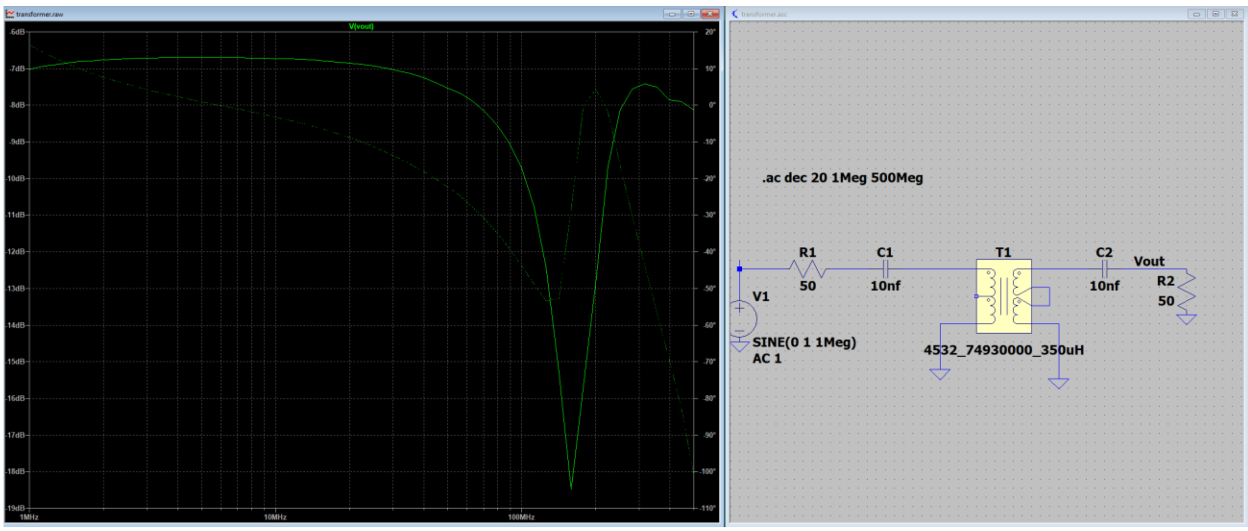

Figure 5 Transformer simulation with LTSpice

It was measured[1] (Figure 6) and found to have 3 dB of loss at 100 MHz and 6 dB at 200 MHz with a 50 ohm load.

[1] -20 dBm signal level was used.

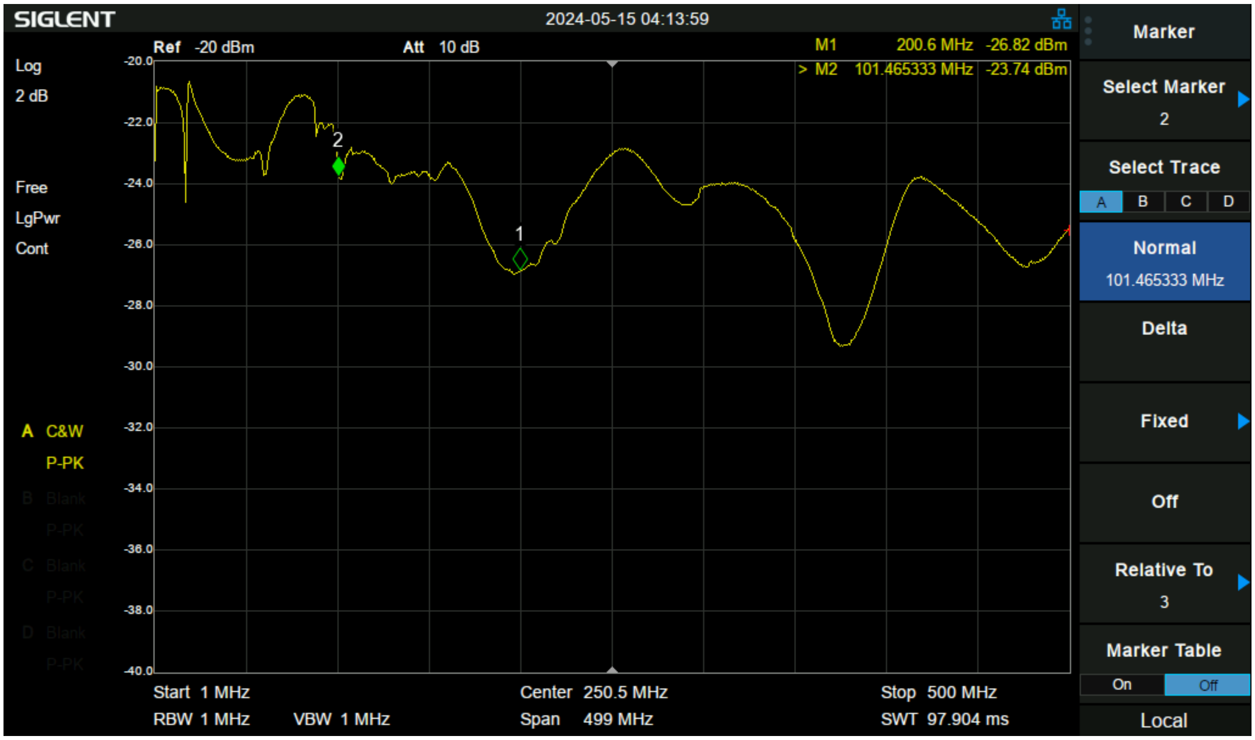

Figure 6 Transformer response with 50 ohm load (analyzer input impedance)

2.1.1 WAIT, ONLY 3 DB?

For starters, if the source generator impedance is 50 ohms and the input impedance is 50 ohms, then the voltage at the input has to be half, or 6dB down. This is correct, but the Spectrum Analyzer already factors that in.

Marker M2 in Figure 6 is −23.74 dBm, so what about the 0.74 dB? That is from cable/connector loss of the fixturing used to measure the transformer[2]; it's possible to save that correction but that was not done here.

Always check your test setup so you know what you're actually measuring!

Here's the fixture loopback measurement:

[2] It does vary a bit with frequency but not enough to worry about relative to the goals of this analysis.

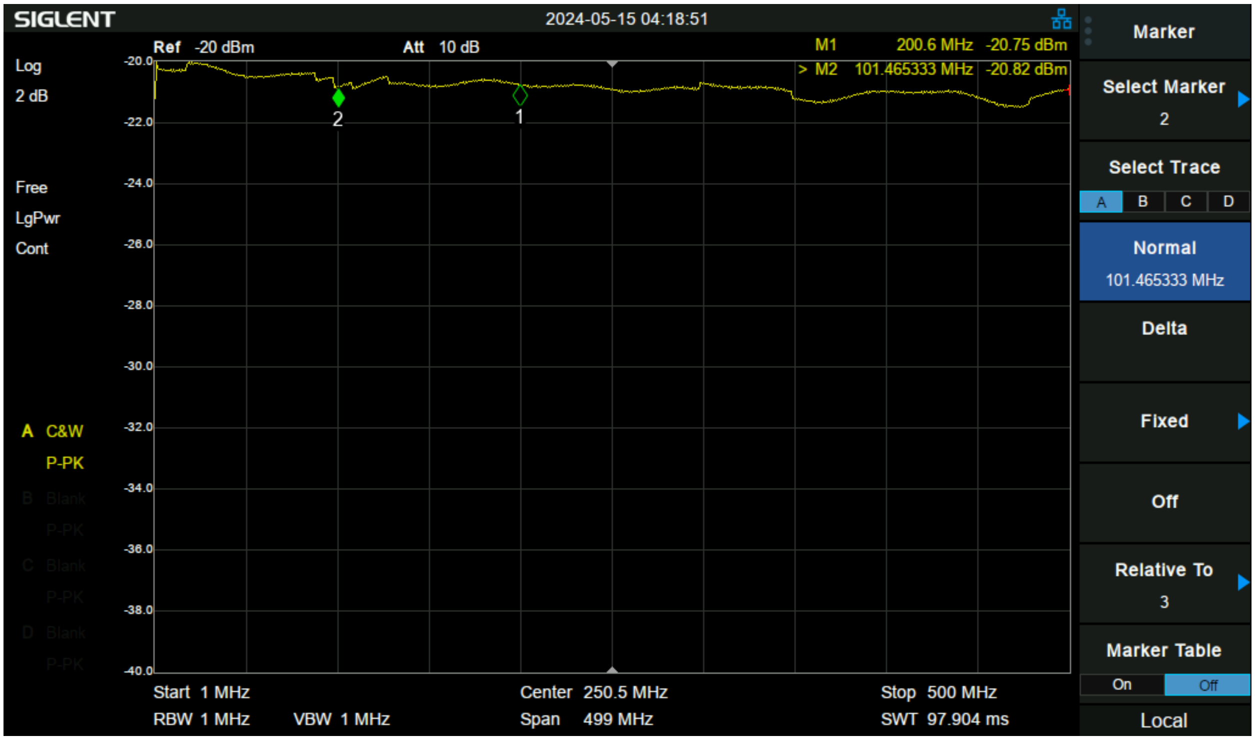

Figure 7 Fixture loopback measurement

2.2 SIMULATION OF THE TRANFORMER DESIGN

More illustrative is an LTSpice simulation of the transformer section wired as it was done in the actual application. The response (Figure 8) is much smoother than the earlier transformer simulation[3] and actually has some resemblance to the measured values in Figure 6 in terms of where there are some loss dips.

[3] We'll leave it to the reader to figure out why this is so different. The first WAG is the grounded center tap has something to do with it. Let us know when you figure it out.

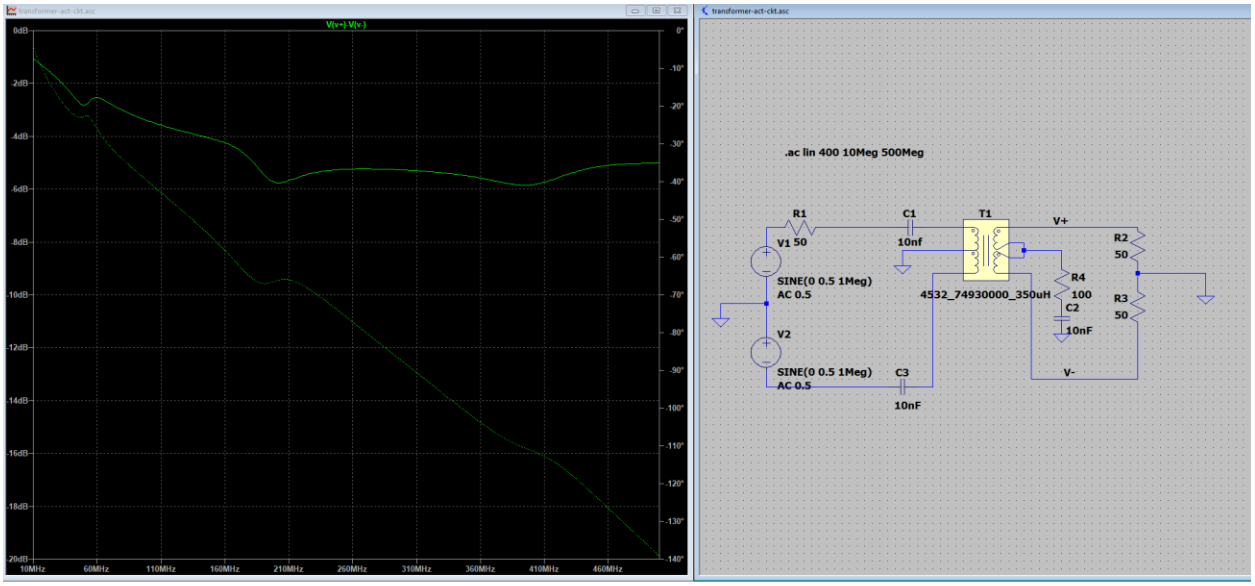

Figure 8 LTSpice simulation with more circuit elements. Linear frequency axis used to match spectrum analyzer plot.

While the loss of signal (3dB to 6dB depending on frequency in the 50 to 200 MHz range of interest) could be problematic at the longest cable lengths it's probably manageable.

2.3 CABLE LOSS?

Belden 1353A is a single twisted pair[4] cable promoted for digital audio and single pair Ethernet. A 36' (11m) length was measured for loss (Figure 9); the losses are on the same order of that from the transformer. With the AD2437 internode distance is specified as 30m max, so as a rough approximation we might say the maximum cable length when using a transformer has been reduced by about a third to 20m.

[4] 24AWG stranded. 100 ohm impedance. Resistivity 26 ohms/1000ft, 84 ohms/1000m.

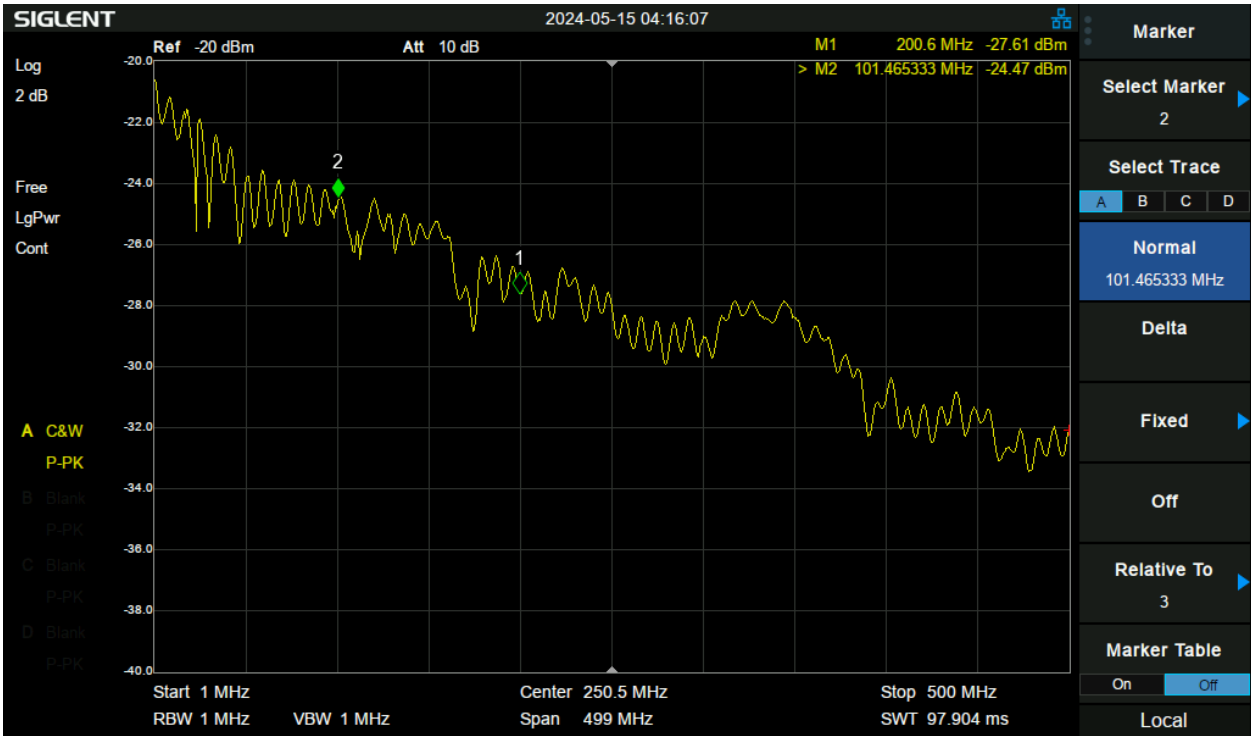

Figure 9 36' (11m) Belden 1353A UTP

3 MEASURED RESULTS

It's reasonably easy to measure the actual A^2B signal with a differential scope probe. Here we used a DIP1400 from NCT Developments (unfortunately no longer available) which has bandwidth over 1 GHz, much more than the 200MHz[5] scope that was used.

The probe was connected to the output of a custom AD2437 module, shown in Figure 10 in a test fixture with a cabled connection (J11) to the upstream board. We therefor would expect upstream data to have slightly higher amplitude than downstream data as the cable between the pictured node and the upstream node will attenuate the signal slightly.

[5] While this sounds problematic, A^2B is designed to cut heavily over 150 MHz so in a correctly designed system the transceiver is not going to see higher frequencies and the scope view can be considered a reasonable match to the chip's input. Higher frequency signals can certainly show up on the A^2B connection, and if chasing EMI/EMC issues full bandwidth measurements could be required.

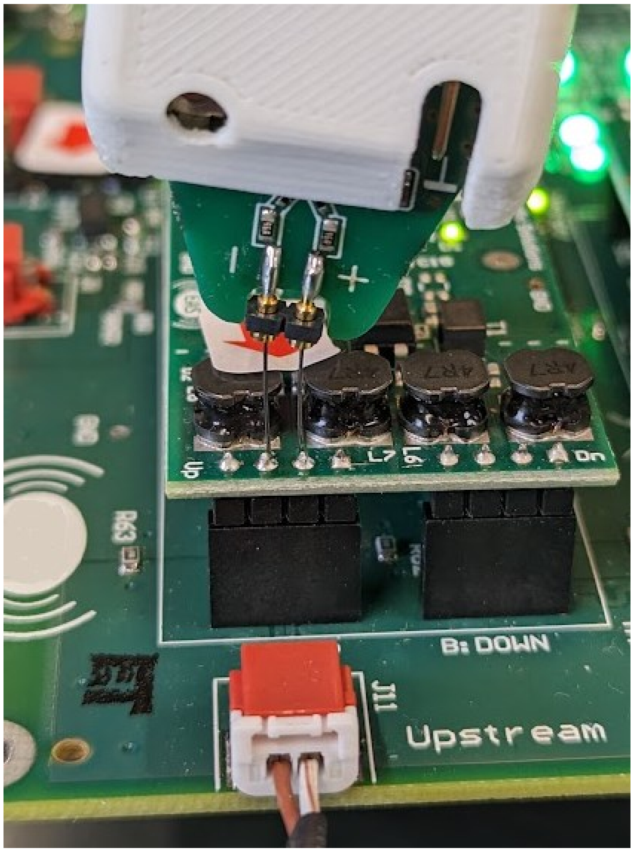

Figure 10 Probe detail/measurement point

Looking at Figure 11 this is exactly what we see, the upstream data is a little higher in amplitude because we're measuring it close to the transmitter.

In standard A^{2}B systems the presence of downstream nodes (connected to the transceiver's B port) will not affect the signal between the transceiver's A port and the upstream node. However in this application there is a DC path from the nodes A to B side to pass power through. The non-zero impedance of the 4.7 uH inductor and the parallel capacitor are all going to load the bus in the nominal 10 - 200 MHz bandwidth that is needed for A^{2}B operation. See Figure 2 for a diagram that shows a summary of the circuit in question, or section 5 for the actual schematic.

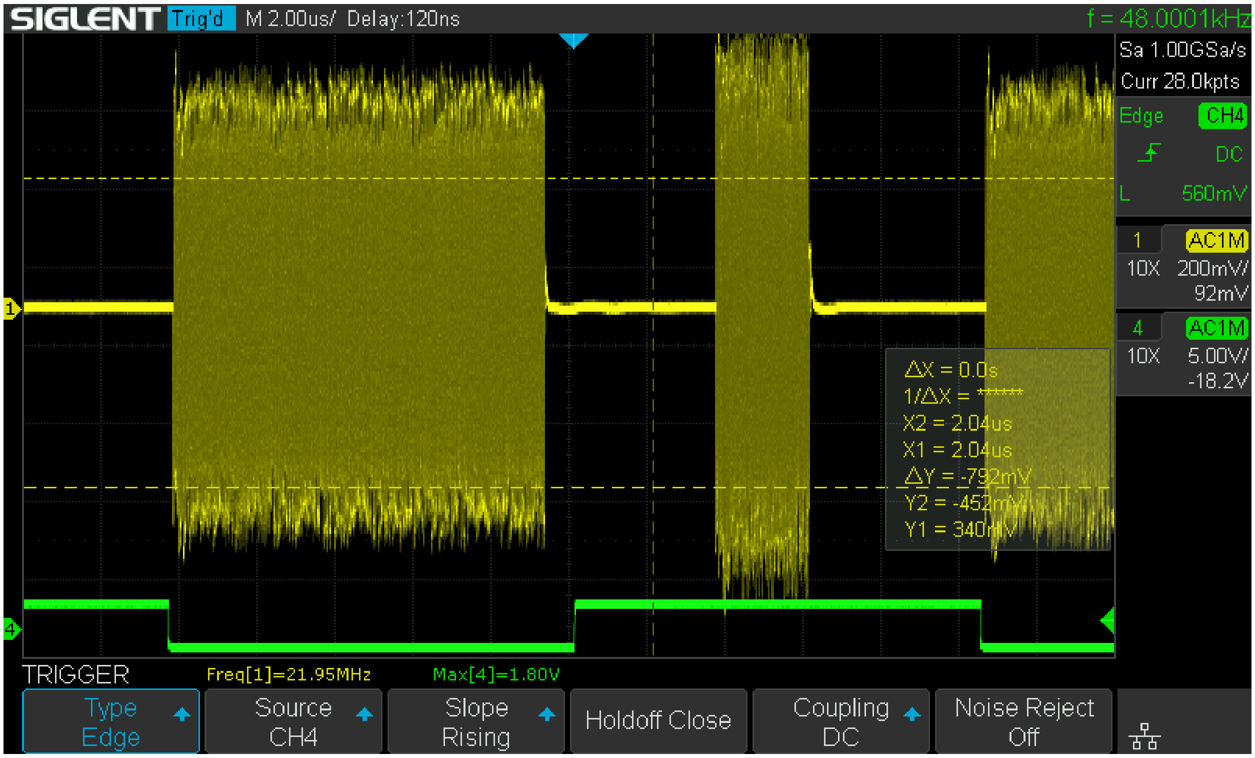

Figure 11 Port A data (yellow) and Frame Sync (green). Upstream data when FS high. No downstream nodes connected.

The dashed yellow measurement lines represent 800mV of amplitude.

It's also instructive to look at the signal integrity. A complication with A²B is the clock used for data generation changes between upstream and downstream; here the scope is triggered on the local I²S frame sync which operates in the upstream clock domain. Unfortunately, A²B is known for very high clock jitter, so when using a simplistic setup with the local frame sync the downstream data is going to look very jittery when viewed with a general purpose scope vs. more specialized ones that would capture an actual eye diagram by locally recovering the clock from the data.

For example here's (Figure 12) the upstream data from Figure 11 where the scope's persistence mode can give us an idea of the data jitter that is present as well as waveform amplitudes.

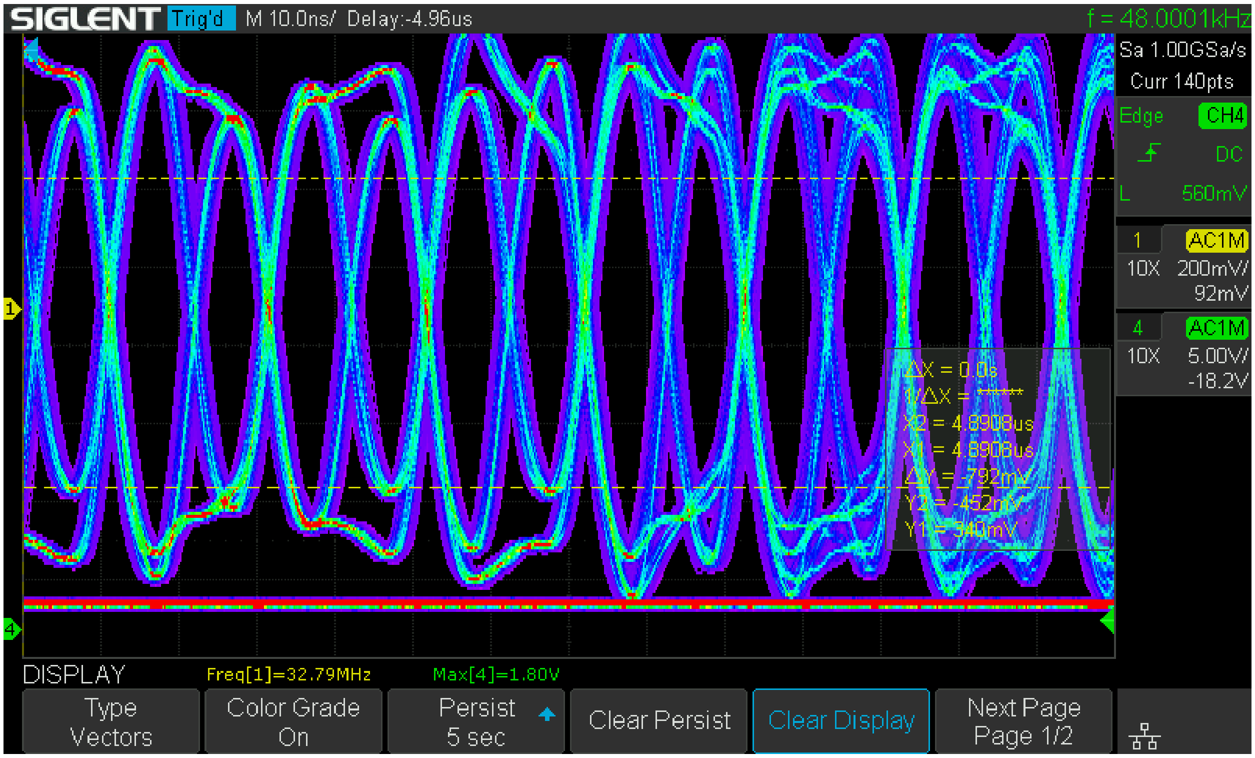

Figure 12 Upstream data (port A) captured using local node as the reference.

By comparison the downstream captured in persistent mode looks awful[6] due to the choice of the reference clock, however we can see (Figure 13) that the waveform is actually fine in terms of transitions and overall shape.

Figure 14 shows a single data capture from the downstream data and it looks quite reasonable compared to Figure 13; we definitely aren't using quite the right test gear but by understanding why we see what we see we can make some reasonable inferences about what's actually happening. For those that have read the earlier Technote on LTSpice simulation of A²B the waveforms reasonably match the simulation results. More importantly, the presence of the isolation transformer does not seem to cause any drastic changes to the waveform.

[6] Though somewhere inside of the AD2437 some PLL is trying to track all of this to create a stable clock for capturing the actual data, though with the Manchester encoding we're just looking for transitions or not, so a different problem than something that has a clock and data latch.

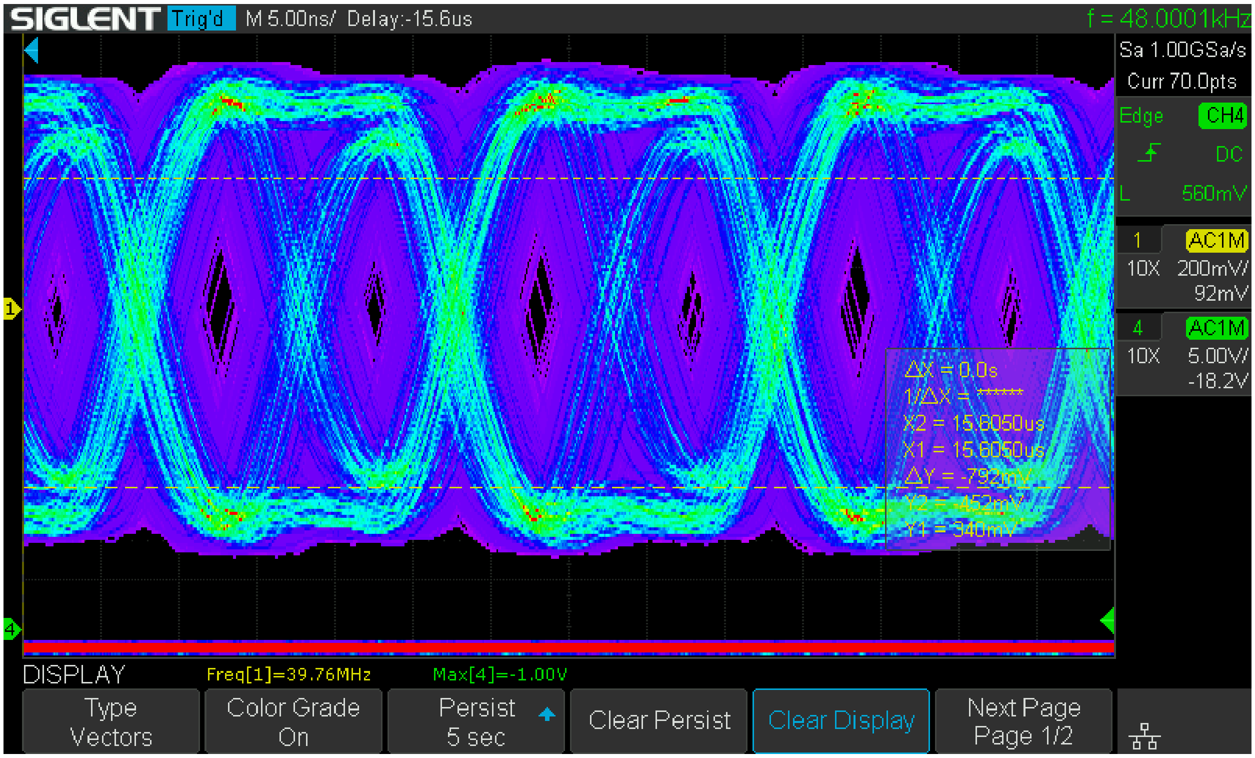

Figure 13 Downstream data (port A side) using the local node as clock reference.

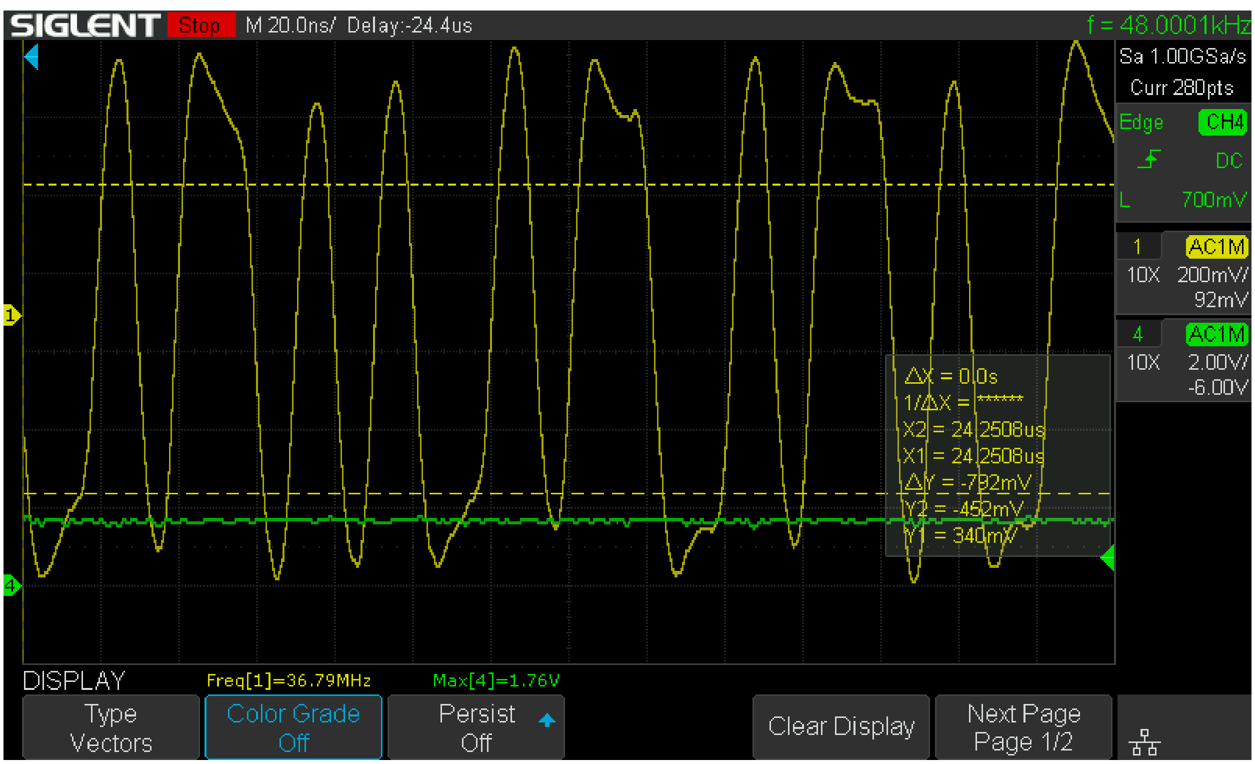

Figure 14 Single data capture.

3.1 WITH 5 NODES

The same captures were made with 5 nodes to see if the extra reactance of the power pass through would affect the A²B signal. The measurements were made at the A port of the 5th node, and the connection to the 4th node was through 20m of cable. The downstream data in Figure 15 is reduced in amplitude from the cable, the loading from the power pass through did not affect the levels when compared with short cables.

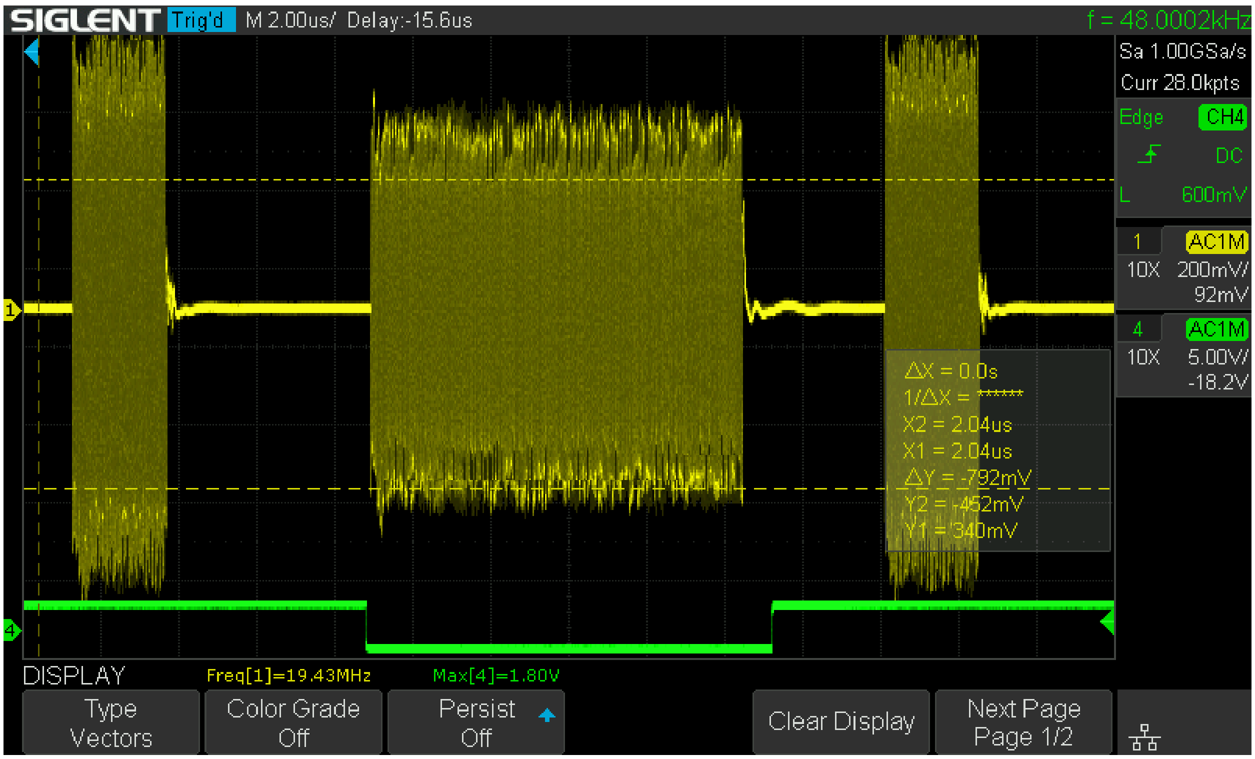

Figure 15 Port A data (yellow) and Frame Sync (green). Upstream data when FS high. Measured at last sub-node of 5 sub-node system .

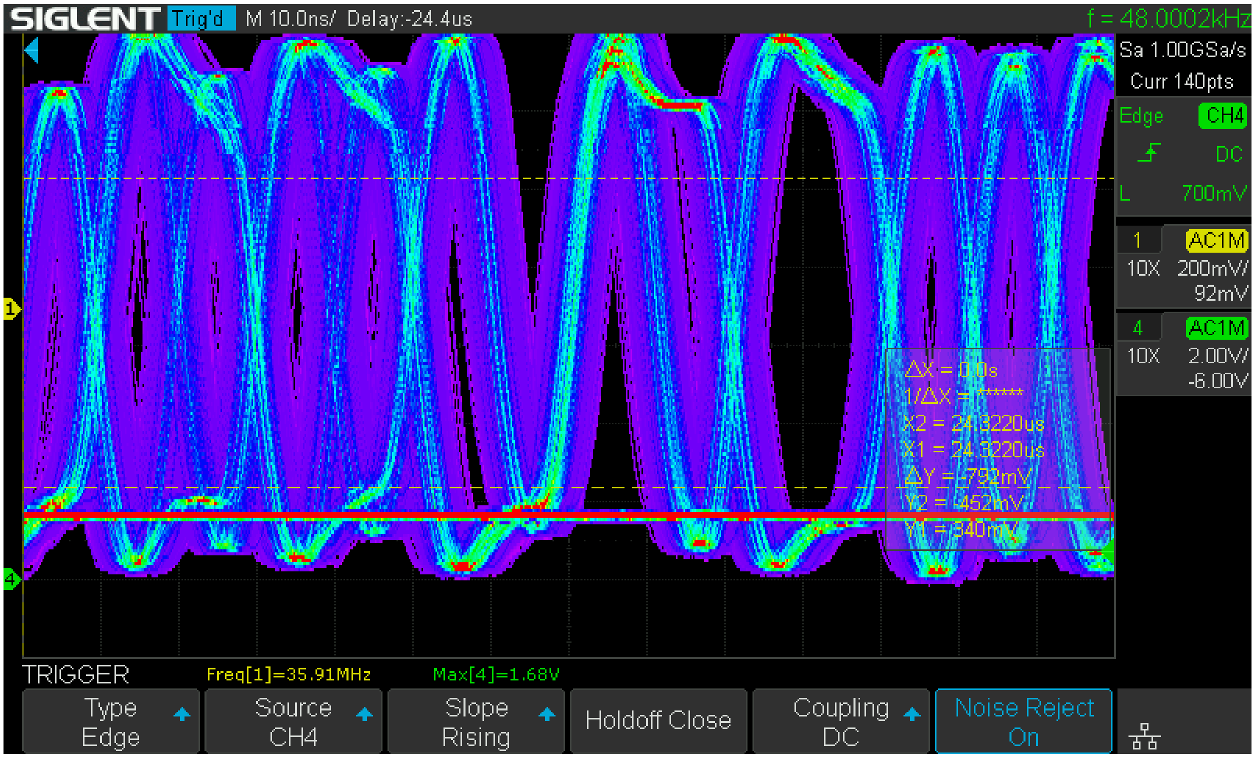

Figure 16 Upstream data from sub-node 5

What's confusing is Figure 16 shows considerable timing jitter yet the reference clock is from the local node. Downstream data is also jittery relative to that local reference (Figure 17).

When these were repeated for 16 nodes the downstream data was actually stable against the local node clock.

While these measurements are a mix of interesting and perplexing, it really doesn't make much difference as there's not anything we can do about the way clocking in the AD2437 works. The LVDS data handling appears robust; our concerns about clock jitter must focus on the effect on ADC and DAC performance, which we've documented in other technotes.

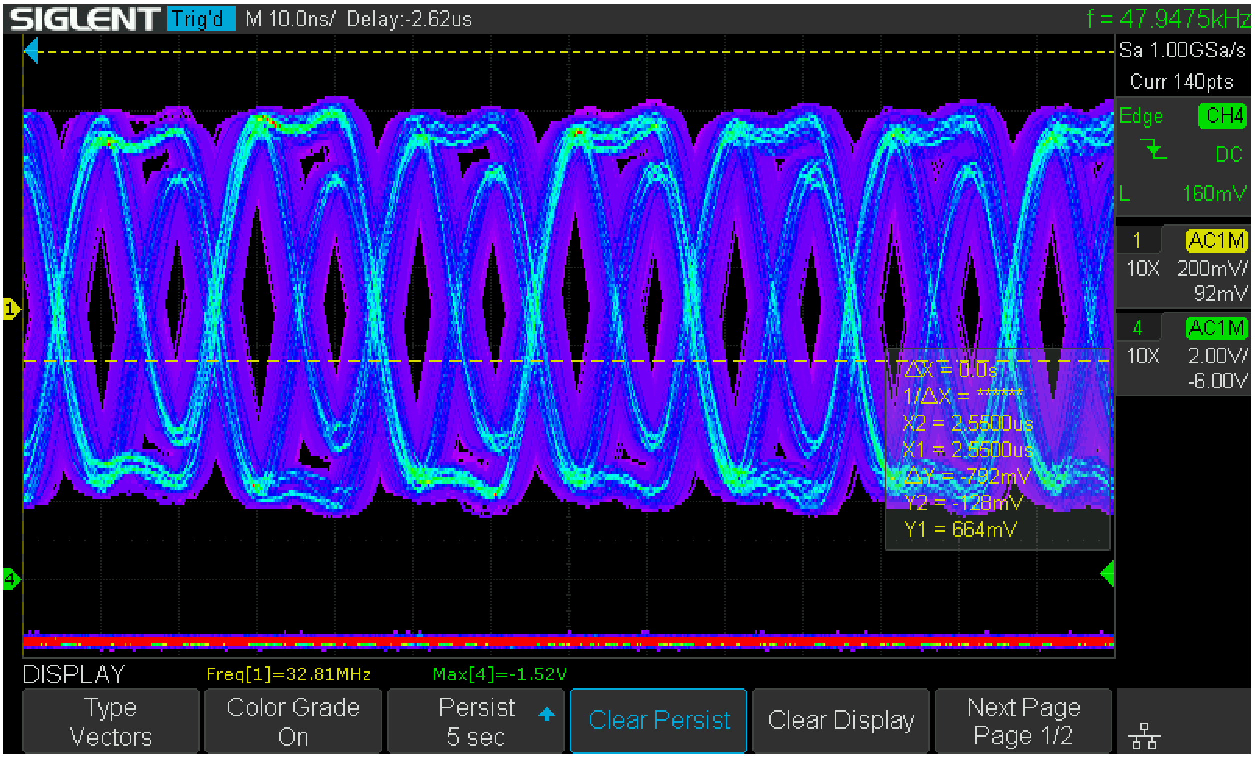

Figure 17 Downstream data at A port of node 5 using node 4 as clock reference.

3.2 A2B SPECTRUM

A picture is definitely worth 1000 words to visualize what's going on. Note there's large low frequency content from the 48 kHz frame period, we can ignore that for looking at the actual LVDS data.

Figure 18 and Figure 19 show measured bandwidth where the BERT test mode is used to generate random data seen in Figure 11.

In Figure 19 the -10 dB point relative to the largest spectral components are marked and we see they encompass from (approx.) 5 MHz to 70 MHz. A^{2}B is designed to limit harmonics found in typical digital signals so that unshielded cable can be used. There is some signal at the 3rd harmonic but 20 dB down from fundamental.

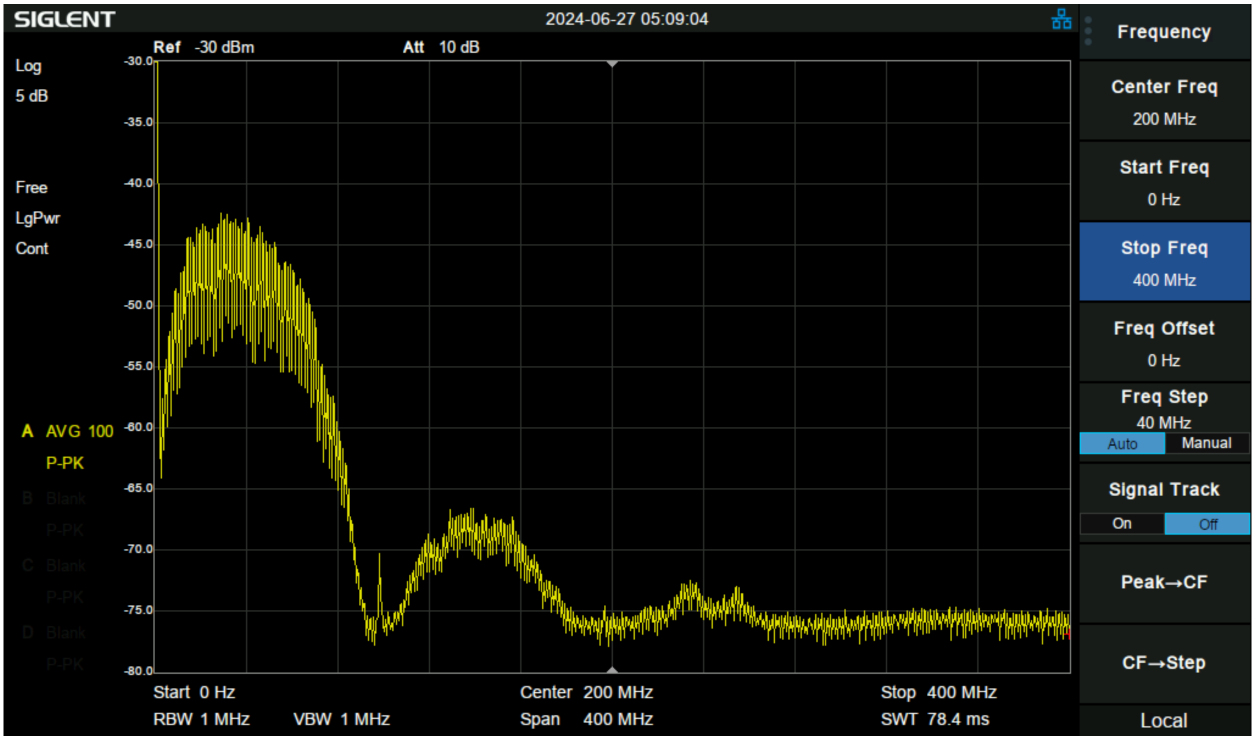

Figure 18 A2B spectrum (random data) 400 MHz bandwidth (100 averages)

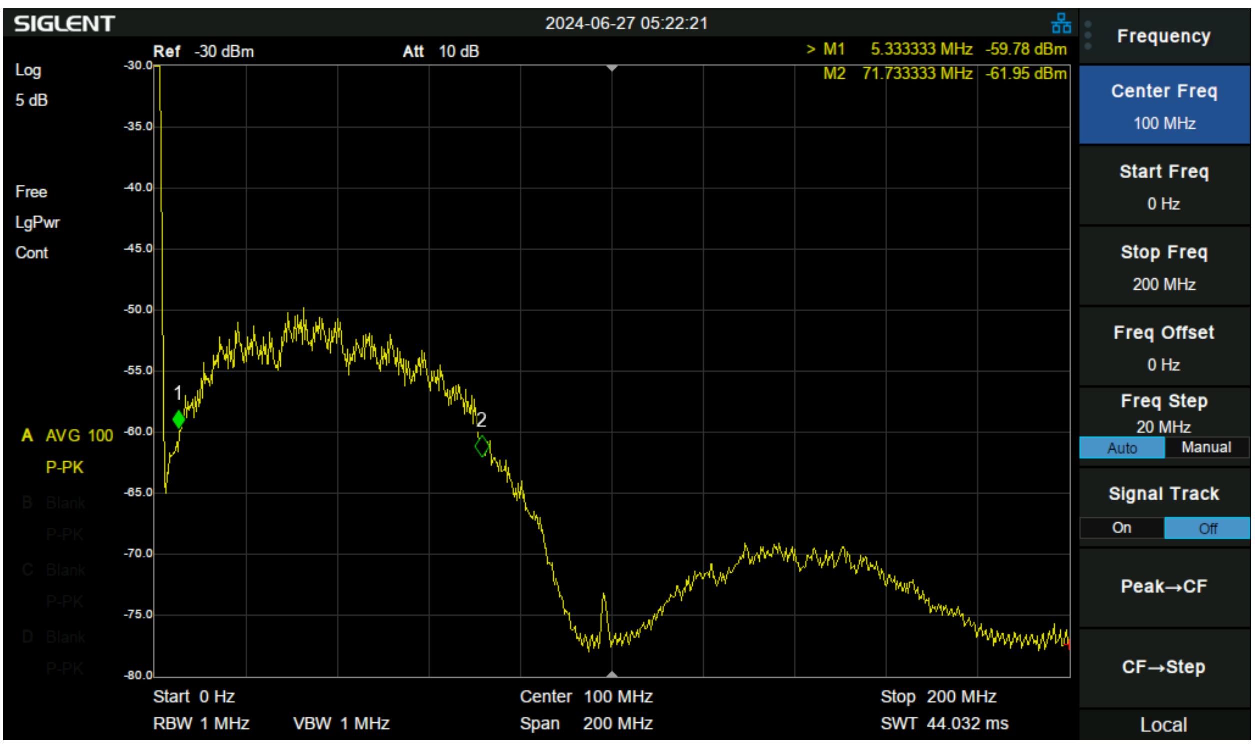

Figure 19 A2B spectrum with markers at −10dB (approx) points, 200 MHz bandwidth

4 FINAL THOUGHTS

Despite the equipment limitations in capturing waveforms we can be reasonably certain that the unique 2 wire bus power scheme and the use of a transformer for galvanic isolation will not create problems for reliable operation. To be conservative we might allow that the maximum internode distance be reduced to 20m, but there are a lot of other factors that could change that for the better (higher quality UTP) or worse (high noise environment).

5 ACTUAL SCHEMATIC