OEM A²B MODULE AND EVM KIT USER MANUAL

For Revision 1 hardware

Rev 1.2

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Products covered:

AB0003 OEM A²B to I²S module (local or bus powered)

AB0106 I/O module (A²B client node, local or bus powered)

AB0108 I/O module (A²B root node, local powered, external BLCK and SYNC)

AB0110 I/O module (A²B root node, local powered, BLCK and SYNC generators)

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Note: This manual covers both current and upcoming revisions of the hardware. 3D board renderings have been used in places where new photos are needed.

INTRODUCTION

1

The Clockworks OEM A²B module AB0003 allows developers to quickly integrate Analog Device's A²B capability in to both prototyping and production environments needing a different connector than the DurClik connector used on all A²B development systems. The AB0003 module provides a quick time to market solution without need to design and debug the A²B portion.

Based on component stuffing options, the module's PCB design supports operation as either an A²B root node or client node. There are two versions of the module, one for locally powered and the other for being powered by the A²B's phantom power. In the case of phantom powered operation the carrier board needs to implement a portion of the required phantom power circuit. The module provides power to downstream A²B client node nodes using A²B's phantom power feature.

The A^2B module is a small 2 layer PCB with two 12 pin 2.54 mm (0.1") and two 4 pin 2.54 mm (0.1") connectors on the bottom for easy mating to other hardware.



Figure 1 OEM A²B module – locally powered version (AB0003L)



Figure 2 OEM A²B module - phantom powered version (AB0003P)

1.1 EVM KITS FOR A²B MODULE DEVELOPMENT

Clockworks offers three modules than can mate with the AB0003 to provide easy access to the module's I/O signals. I²S signals are buffered to facilitate a cable connection. All of these boards can be purchased separately, the EVM kits are provided as a convenience to have a single part

number to order to get everything needed to create functional A^2B nodes. There are four valid combinations of boards that make up the EVM kits.

Kit part number	A2B module	I/O board	Power	Node type	Notes
EVMA2B03SP	AB0003P	AB0106P	Phantom (A ² B)	Client node	
EVMA2B03SL	AB0003L	AB0106L	Local	Client node	AB0106L can also operate as Phantom version (jumper change). Kit includes 9V DC supply.
EVMA2B03MX	AB0003L	AB0108	Local	Root node	Requires external SYNC to operate. Kit includes 9V DC supply.
EVMA2B03ML	AB0003L	AB0110	Local	Root node	Includes local BLCK osc. and divider for SYNC for cases where I ² S not used on root node or attached ADC/DAC does not provide clock signals. Kit includes 9V DC supply.

This manual covers the AB0003 module and its use in the four EVM configurations as they share many similarities. This document also serves as the user manual for the AB0106, AB0108, and AB0110 modules. Further details of the AB0106, AB0108, and AB0110 modules can be gained from the schematics, which are attached to this document, and full design sources are posted on the Clockworks website.

1.2 SOFTWARE SUPPORT

A²B software is supplied by ADI directly at no charge. This software includes both an add on for Sigma Studio that allows an A²B network to be described graphically, and a library with a standard API that can be used by the (host) processor that is connected to the A²B root node (first) node device.

The A²B API information can be found in the ADI document "AD2421/AD2422/AD2425 Automotive Audio Bus A²B Transceiver Programming Reference" document 82-100128-01, Rev 1.1 or as updated to the latest version. This guide, along with the AD2428 A²B transceiver

datasheet, is needed to understand the register settings that are exposed in the A²B add-on for Sigma Studio.

When using ADI's tools for A^2B configuration and operation remember to set the A^2B device type for the module node to AD2428.

Please see section 6 for an example with the A²B add-on for Sigma Studio.

$1.3 \ 1.8V = 1.9V?$

There's some inconsistency on the way the lower of the two I/O voltages available from the AD2428 are labelled. While generally called the 1.8 volt supply, the actual voltage out of the AD2428 is 1.9V and is referenced that way in some places.

2 GETTING STARTED WITH THE BOARD KITS

The setup steps are similar between the versions (A^2B root node or client node/local or bus power) of the EVM configurations.

The I/O board and the modules are ESD sensitive and must be handled following good ESD practices with a proper and safe grounding of the work area and anyone handling the boards.

The EVM kits for local power ships with a 9V DC power supply that has universal input. The North America version uses the two blade plug, where as the international version of the kit has multiple adapters that mate with the supply.

If using the international version of the kit please attach the correct AC mains adapter to the supply.

The AC adapter supplies 500 mA at 9 VDC (center positive) via standard 2.1mm barrel connector. Alternately the boards (except the AB0110) can be powered from a bench supply providing 5 – 9V DC by connecting wires to the Phoenix block connector.

2.1 CONNECTION STEPS - AB0106L CLIENT NODE EVM CONFIGUATION, LOCAL POWER

The EVM kits are shipped with an A²B module installed. This section describes the EVMA2B03SL EVM kit, which consists of AB0003L and AB0106L modules where a local 9V power supply is used.

Connection of I^2S or I^2C is discussed separately in later sections. We suggest for initial testing to not connect any external hardware.

The A^2B module when shipped as part of the an EVM kit with the AB0106 is configured for IOVdd of 3.3V. Some other EVM configurations use IOVdd of 1.8V. For more information please see section 4.3.1.

Setup steps:

- Connect the A²B Root node to your development PC through a USBi emulator.
- Optional: Connect/configure any other A²B client nodes
- Optional: If you've used the AB0106L in a different configuration, verify the power jumper J5 is in the factory default position for local power. (Figure 4).
- Connect an A²B cable to lower module jack ("From Root node") to the B port of the A²B root node or A²B client node located electrically closer to the A²B root node.
- If an A²B client node is used downstream, connect an A²B cable to the lower module jack ("To Client node") to the A port of the A²B client node.
- Connect the A²B Root node board's power
- Power the other A²B devices.
- Attach the 9 VDC supply to AB0106L input jack and plug the supply in to the AC mains.
 - o DO NOT CONNECT A 12V SUPPLY YOU WILL RELEASE THE SPECIAL SMOKE!



Figure 3 AB0106L external connections for local powered A²B client node (AB0003L module not shown)



Figure 4 Jumper set for local power

At this point you should be able to download and execute an A²B network configuration from the host PC via SigmaStudio.

2.2 CONNECTION STEPS - AB0106P CLIENT NODE EVM CONFIGUATION FOR PHANTOM (BUS) POWER

The EVMA2B03SP EVM kits are shipped with an A²B module installed. This section describes an AB0003P module and AB0106P module combination. The upstream A²B node supplies power in this configuration. You must ensure the upstream node can supply power to all of the phantom (bus) powered nodes that are downstream from it (up to the next downstream client node node that's local powered). Review the ADI documentation on bus powered operation if you're not familiar with this.

Connection of I^2S or I^2C is discussed separately in a later section. For initial testing it's suggested to not connect any external hardware – less chance for things to go wrong.

The A^2B module is configured for IOVdd of 3.3V. Some other EVM configurations use IOVdd of 1.8V. For more information please see section 4.3.1.

Setup steps:

- Connect the A²B Root node to your development PC through a USBi emulator.
- Connect the A²B Root node board's power
- Optional: Connect/configure any other A²B client nodes
- Optional: If you've used the AB0106P in a different configuration, verify the power jumper J5 is in the factory default position for phantom power. (see Figure 6)
- Connect an A²B cable to lower module jack ("From Root node") to the B port of theA²B root node or A²B client node located electrically closer to the A²B root node.
- If an A²B client node is used downstream, connect an A²B cable to the lower module jack ("To Client node") to the A port of the A²B client node.
- Power the other A²B devices.
- Attach the 9 VDC supply to AB0106P input jack and plug the supply in to the AC mains.
 - DO NOT CONNECT A 12V SUPPLY YOU WILL RELEASE THE SPECIAL SMOKE!



Figure 5 AB0106P external connections for phantom (bus) powered A²B client node (AB0003P module not shown)



Figure 6 Jumper set for phantom (bus) power

At this point you should be able to download and execute an A^2B network configuration from the host PC to the root node and across the A^2B network via SigmaStudio.

2.3 CONNECTION STEPS - AB0108 ROOT NODE EVM CONFIGUATION LOCAL POWER WITH EXTERNAL BCLK AND SYNC

The EVMA2B03MX EVM kits are shipped with an A^2B module installed. This section describes an AB0003L module and AB0108 module combination where a local 9V power supply is used,

Connection of I^2C is discussed in detail in a later section. There are some specific things to keep in mind for the I^2S connection.

In this EVM configuration an external source must provide the SYNC (48 kHz normally) signal that the AD2428 requires to operate. This signal can not be applied until the external host system has enabled the AD2428 to operate in root node mode. If using Sigma Studio for loading and operating the A²B network there must be some coordination to the setting of the root node mode, the application of the SYNC signal, and waiting for the AD2428 to become ready (about 10 msec) before sending further commands. Details of the AD2428 root node mode startup sequence are found in the ADI AD242x Technical Reference Manual.

The AB0108 includes a PCA9536 4 bit I²C port expander at address 0x41. IO0 is a red LED labeled Host and is useful for verifying I²C connectivity. IO1 is connected to the buffer's enable signal, which is active low. LED D3 (labeled Run) will turn on when IO1 is low. This allows Sigma Studio or other I²C host to control the SYNC signal as part of the AD2428 master mode startup sequence.

The A^2B module when shipped as part of the an EVM kit for the AB0108 is configured for IOVdd of 3.3V. Some other EVM configurations use IOVdd of 1.8V. For more information please see section 4.3.1.

Setup steps

- Connect the external I²S (SYNC) source to the I²S header.
- Connect the USBi to the USBi header.
- If the SYNC source is controlled from I²C connect the SDA, SCL, and ground to your source for the SYNC signal.
- Connect downstream A²B nodes as needed.
- Power up the other portions of the system
 - \circ the AB0110 can be powered up concurrently if desired

- Attach the 9 VDC supply to AB0108 input jack and plug the supply in to the AC mains.
 - DO NOT CONNECT A 12V SUPPLY YOU WILL RELEASE THE SPECIAL SMOKE!
- If an external host processor is handling the initialization sequence, it should:
 - \circ Write the root node mode bit on the AD2428 control register
 - Turn on the SYNC (48 kHz) clock and enable IO1 as an output on the I^2C GPIO expander (chip address 0x41) and set it low.
 - o Wait 10 msec
 - Proceed with initialization as described in the AD242x documentation
 - Sigma Studio can attach to an already running network, the host processor should not try and interact with the system after initialization.
- If using SigmaStudio
 - The schematic must include a way to control the SYNC signal as presence of SYNC causes the AD2428 to execute its internal startup and once that occurs the mode can not be changed to root node.
 - See the examples for how to control the GPIO expander with a startup .xml sequence.

If no I²S data is needed then the external source only need supply SYNC.

2.3.1 BUT THE AD2428 TRM SAYS...

That SYNC can't start until after the AD2428 is put in Master mode via writing to the A2B_CONTROL (0x12) register. However it seems to work as long as SYNC is *not* present for the internal timeout period then the AD2428 will reset itself and wait for the A2B_CONTROL write, which is a much more sane thing to do than having to futz with clock startup timing.

💀 pca9356_run.xn	nl					x
🗋 🖆 🗐 😽	X B B (Ð 😺				
Mode 0	Mode	Address Wid	Address	Data Widt	Data Co	Data
Those o	Write	1	0x03	1	1	0x00
	Write	1	0x01	1	1	0x00
	DELAY			1		0x10
	Write	1	0x01	1	1	0x02
	•					+

Figure 7 I²C Sequence to enable AD2428 to be initialized in A²B Master mode



Figure 8 AB0108 external connections for local powered A²B root node (AB0003L module not shown). The AB0110 has these same connections.

2.4 CONNECTION STEPS - AB0110 ROOT NODE EVM CONFIGUATION LOCAL POWER WITH BCLK AND SYNC GENERATION

The EVMA2B03ML EVM kits are shipped with an A^2B module installed. This section describes an AB0003L module and AB01110 module combination where a local 9V power supply is used.

See Figure 8 for the connectors on the AB0110, which are the same as the AB0108 connectors except the BLCK and SYNC signal directions are opposite, e.g. they are outputs on this board and inputs on the AB0108. The AB0110 also has an MCLK output, so the I²S connector is 14 pins instead of 12 pins. Yeah, well, OK, so they're not really the same.

Connection of I²C is discussed in detail in a later section. I²S SYNC and BCLK are generated on the AB0110 board. A 12.288 MHz oscillator creates a BLCK that would be used for TDM8 mode for 48 kHz 32 bit data, i.e. 8x32x48 kHz = 12.288 MHz.

A jumper (Figure 9) can be set on the AB0110 to select TDM8, TDM4 (6.144 MHz BCLK), or TDM2 (3.072 MHz) operation.



Figure 9 BCLK frequency/TDM size select jumper

The AB0110 include a PCA9536 I²C GPIO expander at address 0x41. A red LED is connected to IO0 (0 = on, 1 = off), and IO1 connects to the enable signal of the 12.288 MHz oscillator (0 = off, 1 = on). These two pins should be programmed as outputs. The green Run LED will light when the local oscillator is enabled to allow generation of BCLK and SYNC.

Setup steps:

- Optional: if using root node node with attached I²S devices:
 - The default configuration is for TDM2 mode for I²S operation. If a different mode is needed change the BCLK select jumper to TDM4 or TDM8 as shown in Figure 9
 - \circ connect external ADC and/or DAC to the I²S header.
- Connect the USBi to the USBi header.
- Connect downstream A²B nodes as needed.
- Power up the other portions of the system
 - the AB0110 can be powered up concurrently if desired
- Attach the 9 VDC supply to AB0108 input jack and plug the supply in to the AC mains.
 - o DO NOT CONNECT A 12V SUPPLY YOU WILL RELEASE THE SPECIAL SMOKE!
- Turn on the SYNC (48 kHz) clock and enable IO1 as an output on the I²C GPIO expander (chip address 0x41) and set it low.
- Wait 10 msec
- Set IO1 on the I²C GPIO expander high. The Green RUN LED will light.
- Proceed with initialization as described in the AD242x documentation

- Using SigmaStudio
 - The example schematic includes control of the I²C GPIO expander to turn on the LED and enable the oscillator when the download step occurs.

2.4.1 BUT THE AD2428 TRM SAYS...

Go back and read 2.3.1, it's important to keep the control of SYNC issue in mind designing your own hardware.

2.5 PUSHBUTTON SWITCH

The AB0106 board includes a pushbutton switch that connect to the A²B module IO7. A small capacitor is used to aid in the debounce of the switch but software should verify a clean switch closure and release.

2.6 AD2428 CONTROLLED LEDS

All of the mating EVM boards offer a LED connected to the AD2428's GPIO. This is convenient during initial setup to validate the network is established in the expected order.

On the AB0106 the LED is connected to IO0, on the AB0108 and AB0110 the LED is connected $IO7.^{1}$ On all of these it is directly connected to the GPIO pin so that 0 = off and 1 = on.

2.7 USE

 $A^{2}B$ evaluation involves at least two nodes, the root ($A^{2}B$ master) node and one or more client ($A^{2}B$ slave) nodes. The examples presented here use the Clockworks module for the root and client nodes, but substitution of other nodes is easy enough.

Please see sections 5, 6, and for examples with the A²B add-on for Sigma Studio. Guidance for direct software development is included with the ADI API documentation.

¹ We agree that consistency here could have been better.

2.8 I²S CONNECTOR

There are two version of this connector, a 14 pin one as described in Table 1 for the AB0106 and AB0110 modules and the 12 pin version as described in Table 2 for the AB0108.

3 EVM DESIGN INFORMATION

The three boards (AB0106/0108/0110) that combine with the AB0003 OEM A^2B to I^2S module are very basic in function and intended to be easy to modify during initial system prototyping. Larger 0805 SMT components and .1" (2.54mm) connector spacings are preferentially used.

When the EVM configuration is purchased a design package is provided by email or an emailed link to download the information from the website will be provided.

The package includes the following information for AB0106, AB0108, or AB0110 boards:

- PDF of schematic. Part information is embedded in the PDF, click on a part symbol to see detailed information on the part.
- 3D PDF of the board. Note that Acrobat Reader security will ask if you trust the document.
 You must click yes. You then may need to click in the blank field to make it display. Some versions of Reader have a bug and will not display unless the document is saved locally.
 You can enable display of various board features and components using the standard 3D Acrobat features.
- Zip with Gerbers.
- Altium project files
- BOM as an Excel spreadsheet
- .STEP file for the A²B module

3.1 POWER INPUT

The AB0106, AB0108 and AB0110 design include a diode on the DC input to prevent damage from a reverse connected input supply. This diode also reduces the input voltage by about 0.4V; on the board/schematic this is rounded off to call the supply an "8V" supply; the actual voltage is about 8.6V.

The AD2428 maximum supply voltage is 9V and this small extra drop prevents operating the AD2428 on the module near its limit. The module design includes a Schottky diode as suggested by ADI's design guide² for a local powered A²B module, meaning there is another 0.4V or so drop on the A²B module and this the actual voltage to the AD2428 on the module is about 8.2V.

The only possible impact from the lower supply voltage is if A²B phantom power feature is used to power multiple downstream client node nodes; each node has a 0.4V drop. For more details please see the full AD2428 datasheet for a discussion on phantom power of client node nodes.

The AB0106, AB0108, and AB0110 use the IOVDD output by the AD2428 for the I²S buffer. The I2C expander (AB0108 and AB0110) and the oscillator and divider (AB0110) are likewise powered by the AD2428's IOVDD.

The A²B module must be jumpered for 3.3V IO when used with any of these three boards.

The user LED is connected to ground so relies on the AD2428 to source its power, which is set for about 1.5 mA to both keep the brightness low and power draw minimal.

The other LEDs on the AB0108 and AB0110 (Run, Host) are also powered by the AD2428's IOVdd.

3.2 FEATURES FOR MODIFYING THE EVM

There may be cases where a change to the default wiring is needed. There are provisions in the design to attempt to simplify making modifications. Please note that Clockworks can not support modified boards nor take any responsibility for your modifications making your clothes shrink in the dryer or something worse like crashing your car in to a light pole.

3.2.1 TESTPOINTS

Testpoints are available on some of the signals to facilitate probing or modifying the board. Please see the schematic for their (electrical) location.

² In part this protects against backwards phantom power flow to unpowered nodes or in cases of a power to bus short.

3.2.2 NT COMPONENTS

NT (Net Tie) components are 0603 footprints with copper trace between them. By cutting the traces the two net pieces can be isolated and connected to different places. Please see the schematic for the board for the functions they enable.

3.2.3 EEPROM

The AB0106 (rev 2 and later) includes a footprint for a SOIC-8 (150 mil) 8 pin EEPROM. The EEPROM is installed by default on the local powered AB0106L version, a 32Kx8 part is used and typically resides at I²C address 0x50. PCB traces/pads can be cut/jumpered to change this address.



Figure 10 EEPROM location on AB0106 (rev 2)

Parts like Microchip's 24AA256T-I/SN or STMicro's M24256-BRMN6TP can be installed here. C16 is a 100nF decoupling capacitor. The three NT jumpers can be used to modify the default base address.

3.3 AB0106 CLIENT NODE MODE BOARD (EXTERNAL CLOCK)

In addition to the four mating connectors for the AB0003 described in Section 4.1, there are two signal connectors on the backside³ of the AB0106.

3.3.1 EXTERNAL CONTROL CONNECTOR AB0106

This 6 pin connector is a TE MTA-100 series part, 640456-6. It follows the same pinout as used on some other Clockworks products. Pin assignments are as follows:

³ When mated to the AB0003 module the "backside" is opposite the component side of the AB0003.

1	GND
2	SDA
3	GND
4	SCL
5	3.3V
6	RESETn

The RESETn is normally defined as an active low signal that is driven by open collector logic where the default driving source includes a pullup. On the EVM board and the A²B module there is no reset capability, the parts have built in brown-out and reset. Therefor this signal serves no purpose for normal EVM use.

If using the I²C bus keep in mind that the AD2428 device on the A²B module in client node mode is normally the I²C root node.

This connector is not normally installed on the AB0106P bus (phantom) powered module.

3.3.2 AB0106 I²S CONNECTOR

This 14 pin dual row connector (2.54mm/0.1" spacing) provides access to the I^2S signals. It is not installed on the AB0106P bus (phantom) powered module.

The first 12 pins are wired in the same configuration as used on some ADI development boards. MCLK is also brought out, but use of this signal is dependent on the AD2428 programming to enable it and select the frequency ratio between the frame rate and MCLK.

2	BCLK (out)
4	SYNC (out)
6	DTX0 (to DACs)
8	DTX1
10	DRX0 (from ADC)
12	DRX1
14	MCLK (out)
1,, 13	GND (odd pins)

Table 1 AB0106 and AB0110 I²S connector pinout

Except for DRX0 and DRX1, the signal are all outputs and are buffered by a 74LVC2245 buffer; this chip includes series termination resistors to improve signal quality. A receiver chip on the far end may be needed to maintain signal integrity. For bench top use with short lengths of ribbon cable no extra considerations should be needed.

If the DRX0 and DRX1 inputs are used then the source for those signals should likewise be series terminated and have appropriate drive strength for the lengths of cable you plan to use. Remember that the received data is clocked on the AD2428's BCLK. If the attached ADC board buffers the signal keep in mind the shift of data timing relative of BLCK.

3.4 AB0108 ROOT NODE MODE BOARD (LOCAL CLOCK)

In addition to the four mating connectors for the AB0003 described in Section 4.1, there are three signal connectors on the backside⁴ of the AB0108.

3.4.1 EXTERNAL CONTROL CONNECTOR AB0108

This 4 pin .1" (2.54mm) header provides access to the I2C bus and the IRQ pin of the AD2428 when the module is installed. This connector is not keyed. Pin assignments are as follows:

⁴ When mated to the AB0003 module the "backside" is opposite the component side of the AB0003.

1	IRQ/IO0
2	GND
3	SCL
4	SDA

3.4.2 AB0108 I²S CONNECTOR

This 12 pin dual row connector (2.54mm/0.1" spacing) provides access to the I²S signals.

The 12 pins are wired in the same configuration as the first 12 on the 14 pin version on the AB0106 as well as matching ADI development boards that offer this connector.⁵

2	BCLK (input)
4	SYNC (input)
6	DTX0 (to DACs)
8	DTX1
10	DRX0 (from ADC)
12	DRX1
1,, 11	GND (odd pins)

Table 2 AB0108 I²S connector pinout

There is an important difference in the way this connector is used versus the client node AB0106 version described in Table 1. The AD2428 on the root node is fed a clock (the frame sync signal called SYNC) that it generates all of the rest of the system timing from, including the (nominal) 50 MHz embedded clock of the A²B bus.

The SYNC signal is normally 48 kHz but the AD2428 also supports 44.1 kHz. As detailed in ADI's AD242x Technical Reference Manual, the SYNC signal can only be applied after the host has placed the AD2428 in root node mode by writing to the AD2428's control register.

A root node AD2428 expects the bit clock (BCLK) to be an input, though its only use is for clocking in the I²S data. The choice of the BCLK frequency is a function of the TDM mode (2, 4, 8, or 16) used on the I²S lines as well as the datasize (16 or 32 bit) and the data rate (1x, 2x, 4x).

BCLK and SYNC must be synchronous.

⁵ It seems to be the case that some newer ADI boards have removed this connector and replaced it with sets of jumpers

3.4.3 AB0108 USBI CONNECTOR

For use in root node mode without a host processor an emulator (ADI calls it *USBi*) is required for downloading and interacting with the AD2428. For more information please see:

http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boardskits/eval-adusb2ebz.html#eb-documentation

This board only uses the I^2C SDA (pin 3) and SCL (pin 1) lines from the 10 pin .1" (2.54mm) USBi emulator. Ground is on pin 10.

3.5 AB0110 ROOT NODE MODE BOARD (LOCAL CLOCKS)

In addition to the four mating connectors for the AB0003 described in Section 4.1, there are three signal connectors on the backside⁶ of the AB0110.

3.5.1 AB0110 I²S CONNECTOR

This 12 pin dual row connector (2.54mm/0.1" spacing, male pins, shrouded) provides access to the l^2S signals.

The 12 pins are wired in the same configuration as the first 12 on the 14 pin version on the AB0106 and the same signal assignments as on the AB0108 described by Table 2.

⁶ When mated to the AB0003 module the "backside" is opposite the component side of the AB0003.

Table 3 AB0110 I²S connector pinout

2	BCLK (output)
4	SYNC (output)
6	DTX0 (to DACs)
8	DTX1
10	DRX0 (from ADC)
12	DRX1
1,, 11	GND (odd pins)

Like on a the AB0106 client node node configuration. The AD2428 on the root node is fed a clock (the frame sync signal called SYNC) that it generates the rest of the system clocking from, including the (nominal) 50 MHz embedded clock of the A²B bus.

3.6 USBI CONNECTION

For use in root node mode without a host processor an emulator (ADI calls it *USBi*) is required for downloading and interacting with the AD2428. For more information please see:

http://www.analog.com/en/design-center/evaluation-hardware-and-software/evaluation-boardskits/eval-adusb2ebz.html#eb-documentation

This board only uses the I^2C SDA (pin 3) and SCL (pin 1) lines from the 10 pin .1" (2.54mm) USBi emulator. Ground is on pin 10.

4 A²B MODULE INFORMATION

All module functions are determined by the AD2428 device, please refer to that device's datasheet and technical reference manual for detailed operating information.

4.1 CONNECTORS

There are four connectors on the bottom side of the AB0003 module.

4.1.1 PRIMARY SIGNALS

Pinout – A Connector, 12 pin .1" (2.54mm) single row, male pins.

Pin	Name	Notes
1	IOVDD	Jumper selects between AD2428 internal regulator voltages, default is 3.3V (vs. 1.8V)
2	GND	
3	ADR2	AD2428 ADR2/IO2 line with 10K pulldown
4	ADR1	AD2428 ADR1/IO1 line with 10K pulldown
5	IRQ	AD2428 IRQ/IO0 line
6	GND	
7	SDA	I2C data
8	SCL	I2C clock
9	GND	
10,11	Vxx	Power 5-8V suggested range, 4V min, 9V max.
12	GND	

Pinout – B Connector, 12 pin .1" (2.54mm) single row, male pins.

Pin	Name	Notes
1	GND	
2	BCLK	AD2428 bit clock (output from module as a client node)
3	GND	
4	SYNC	AD2428 frame sync (output from module as a client node)
5	GND	
6	DTX0	AD2428 DTX0 with 10K pulldown (output)
7	DTX1	AD2428 DTX1 with 10K pulldown (output)
8	GND	
9	DRX0	AD2428 DRX0
10	DRX1	AD2428 DRX1
11	GND	
12	107	AD2428 IO7/PDMCLK pin

4.1.2 A²B SIGNALS

Pinout – A Port (Upstream) Connector, 4 pin .1" (2.54mm) single row, male pins. AB0108 and AB0110, as a Master node, do not use upstream (A) ports. However the AB0108 and AB0110 boards have this connector installed for mechanical reasons. The AB0003 module, since it can be used as root (Master) or client (Slave) node always has this connector installed.

Pin	Name	Notes
1	GND	
2	Р	A ² B LVDS + side
3	Ν	A ² B LVDS - side
4	GND	

Pinout - B Port (Downstream) Connector, 4 pin .1" (2.54mm) single row, male pins.

Pin	Name	Notes
1	GND	
2	Ν	A ² B LVDS - side
3	Р	A ² B LVDS + side
4	GND	

The LVDS – signal is also the negative rail for phantom power. Phantom powered nodes can not connect their local ground (e.g. the low pass filtered – signal) to any external ground as that will be detected as a fault by the upstream node.

The carrier board should route the A²B signals as a differential pair with 100 ohm impedance. Routing should be symmetrical and follow ADI's guidance.

4.2 MODULE MECHANICAL INFORMATION



Figure 11 A²B module dimensions, top view

The board is slightly asymmetrical relative to the mounting holes, which are 4mm from the back edge and 3mm from the front (A²B connector) edge.

All electrical components are on the top side of the board. The two 12 pin and two 4 pin connectors are located on the bottom side of the board.

Component heights are nominally as follows for the figure shown below. Component substitutions during assembly may sometimes be required; this may alter these values.



Figure 12 A²B module side view cut-away, local powered version.

Board thickness 1.6 mm(.062").

Plastic on bottom connectors thickness 2.29mm (.090").

Pin length 6.1mm (.24").

C33 (bulk 100 uF cap) height 7.7mm (.303")

For the phantom (bus) powered version C33 is not present and the suggested keepout height is 3.5mm (.14")

4.3 INTERFACE DETAIL

The following two schematic sections from the A²B module are provided to aid in understanding the A²B module interface.



Figure 13 Module A connector wiring⁷

C33 is required by the ADI design rules for a local powered node and should be kept in mind for the load capacitance on the external supply. TP10 and TP11 are holes in parallel with the location of C33 to allow a phantom powered AB0003 module to be converted to a local powered one by adding a through hole capacitor. There is also a diode (D4) that must be added (the rest of the circuit is on the standard AB0003P module even though it's not used). It is not present on phantom powered AB0003P modules.

⁷ RefDes for Rev 1 module PCB shown unless noted otherwise.





The other connector carries the I²S signals. Analog Devices suggests series termination and a small 27 pF capacitor to reduce EMI issues and the module implements those suggestions.



Figure 15 Module B connector wiring. On AD2428 IO7 can also be PDMCLK out pin.⁸

The remainder of the module schematic corresponds to the ADI recommended design for locally powered nodes, as that guidance is subject to change please see the ADI documentation for further details.

Unused module pins may be left floating except for the I²C pins. (see 4.3.3).

4.3.1 IOVDD

This pin is normally an output from the module. It can be configured for 3.3V or 1.8V⁹ operation.

If neither voltage selection jumper is installed then IOVdd can be set externally, however all of the AD2428 rules about supply sequencing must be strictly adhered to.

The I²C bus must match the IOVdd, i.e. the pullup resistor's connection to the supply on whatever board the AB0003 plugs in to should have the pullups (2.2 K typical) connected to IOVdd.

⁸ RefDes for Rev 1 module PCB shown unless noted otherwise.

⁹ The datasheet for the AD2428 specified the range of voltage from that supply as 1.7 to 1.98 with 1.9 being the typical value. In a few places though it's referred to as the 1.8V supply.



Figure 16 Rev 1 PCB IOVdd connections. 1V9 is connected to the AD2428W VOUT1, pin 32. 3V3 is connected to the AD2428W VOUT2, pin 29.



Figure 17 Rev 2: IOVdd jumper resistors. 3.3V is the factory default

4.3.2 VXX

It is AD2428 datasheet shows that this pin should not exceed 9V, though the Schottky diode in the module input supply connection does mean that 9.3V is closer to the absolute maximum limit of the module. The minimum voltage is 4.2V for the module to operate, however no phantom power can be supplied at that voltage.

4.3.3 SCL, SDA

As stated on the AD2428 datasheet, these two pins should be grounded if not used by system this board plugs in to.

If I^2C is used then the main board must provide the I^2C pullups and correctly match the IOVdd.

5 CONFIGURATION EXAMPLE WITH SIGMA STUDIO (AB0108 LOCAL POWERED MODE)

This section outlines the steps for using the Clockworks AB0108 I/O module with the AB0003 $A^{2}B$ to $I^{2}S$ module with the Analog Devices $A^{2}B$ add-on for Sigma Studio. ADI includes tutorial examples with the software add-on and this section are generally derived from this ADI provided example:

..\Schematics\BF\A2BSchematics\adi_a2b_3NodeSampleDemoConfig.dspproj

You can also create a new example on a blank sheet Sigma Studio sheet following the procedures in the ADI documentation. When first starting out it may be easier to edit a provided example for your host (and save it as a new file!) than to get all of the settings in place.

This examples assumes the use of the standard ADI A²B EVM root node ('WDZ) board as the A²B root node. There are two versions of this board and they require slightly different settings. The directions here are for the newer AD2428 based WDZ board, if using one of the older boards use one of the ADI example for that as your starting point.

If using the SC589 based SHARC Audio Module (SAM, but also known as the SHARC-mini) there are additional steps to running Sigma Studio. While the concepts are the same as working with the ADI EVMs there are a few differences that must be considered. For a detailed example of the use of A2B with SAM please see the user guide for the Clockworks AB0001 module and EVM.¹⁰ Alternatively Analog Devices supplies considerable documentation for SAM on its Wiki page on the ADI website.¹¹

5.1 EXAMPLE HARDWARE SETUP

This example illustrates how the AB0106 can be used with ADC and/or DAC boards to create quick prototypes of actual system hardware, which in turn allows software development to begin as well as supporting performance testing before committing to specific hardware. Figure 18 illustrates the hardware being used in this example.

¹⁰ https://clk.works/products/a2b-products/a2b-module-evm/

¹¹ https://wiki.analog.com/resources/tools-software/sharc-audio-module

A Clockworks A²B EVM board¹² (without the A2B module) is used for the ADC and DAC functions as its ADAU1761 codec/DSP must be programmed over I²C, which is typical of many boards that would be of interest in this type of scenario.

The 'WCZ board is not required, it is included for consistency with some of the other examples.



Figure 18 Three node example using AB0106L

Figure 19 shows a closer look at the jumpers used between the two boards. Connections are made as follows.

Control header (white 6 pin):

- SDA -> SDA
- SCL-> SCL
- GND->GND

¹² Part number EVMA2B51.



Figure 19 Detail of I^2C and I^2S connections between AB0106 and Clockworks 1761 EVM board

I²S header (AB0106 < -- > EVM):

- GND -> GND
- BCLK -> BCLK
- SYNC -> SYNC
- DT0 -> DACDAT (DR0)
- DR0 <- ADCDAT (DX0)

Other:

• AB0106 I²S header MCLK -> EVM A connector pin 3 (CLK) (yellow wire in Figure 19)

The SigmaStudio schematic, Figure 20, illustrates the example that will be run. Audio from the microphones on the 'WCZ board plays out the EVM board headphone out, audio in to the EVM board plays out the 'WDZ audio output.



Figure 20 Sigma Studio 3 node example for the hardware in Figure 18

Figure 20 shows one of the ADI default examples with the (ADI WDZ board) ADAU1452 root node and WBZ and WCZ client nodes. The Clockworks AB0106 replaces the WBZ client node in this example. If needed, change the chip type on the 2nd node to AD2428 as shown by the red arrow. (later example files are already set for the AD2428 on all nodes).

If you don't have the WCZ microphone board you can delete it from the example. The audio streams will need to be reassigned, for example they could be sent in both directions between the 'WDZ and the AB0106/EVM.

In this example the root node must be programmed, which is enabled by selecting its properties and checking the *Program during discovery* box. The path to the XML file with the ADAU1452 must be valid and if trying the system for the first time should be the default pass through program.

It's suggested to copy the xml subdirectory to your local working directory, along with the SigmaStudio schematics for the default programs. This way the ADI provided examples are never accidentally changed,

Audio Host ADAU1452 Properties
Block Register Read/Write
Peripheral register programming file xml\adi_a2b_master_ADAU1452.xml
Program during discovery Edit Program
SigmaDSP project file (optional) chematics\adi_a2b_master_ADAU1452.dspproj Open Update XML
Generic Register Read/Write
Addr Width Address Data Width Data
Register 1
Results

Figure 21 Root node ADAU1452 properties

The ADAU1761 on the 'WDZ must also have a default program loaded, Figure 22.

Desig	haral graderoming file	umladi alb manter ADAU1761 uml
rent	nierai programming me	
▼ P	rogram during discovery	Edit Program
Sigm	aDSP project file (optional)	
		Open Update XML
Generic	Register Read/Write	
	Addr Width Address	Data Width Data
Register	1 ▼ 0x00 €	1 • Ox00 Read Write
Doculto		E.

Figure 22 ADAU1452 on root node

Æ	A2B Slave	Node1 WB	Z Properti	es			X
	General Vie	W Register \	/iew Strea	am View			5
	-Slave (Config					
	I2C Inte	erface Freque	ency 400	kHz 👻			
	Super	Frame Rate	48.0	0 kHz 👻			
	Node F	Response Cyc	cles Ox7	8			
	Spread	l Spectrum Se	ttings				
	Mode	No Spread		•	Frequency	4x	•
	Depth	Low		🔘 High			
	Config and	d Control Sic	ot Config 4	Audio Config	Rate and ClkOut Inter	rupt Config Pin Config	
	Master Add A-Side Cab	ress le Length (m)	0x68		Bus Address	0x69 ation from EEPROM	₹

Figure 23 AD2428 Properties for Clockworks EVM based on defaults for ADI WBZ board.

Once all of the settings are checked hit the Link Compile Download button and after a few seconds the A²B nodes should turn green to indicate the network has been discovered. Typical errors are unplugged A²B cables, unpowered A²B nodes, or the USBi not plugged in to the PC. Very rarely (one in 100 perhaps) Windows forgets about USB and you'll need to unplug and replug the USBi.

5.1.1 EEPROM CONFLICT

Both the EVM board in this example and the AB0106 have their EEPROM at address 0x50 by default. If you want to experiment with EEPROMs one of them will need to have an address jumper cut and the pin tied high.

5.2 GENERAL I²S SETUP

When connecting the I²S lines to a DAC or ADC you will need to program the I²S settings illustrated in the next figure. Failure modes for wrong settings include no audio, very badly distorted audio, or full scale modulated noise.

Details of the settings are dependent on the hardware you connect. Pay close attention to which BCLK edges are used for outputting and sampling data; they should be set of the opposite edge between the sending and receiving side of an I²S data line.

AD242x Slave - A2B EVM 0 Properties					
General View Register View Stream View	9				
125					
TDM Mode TDM2 -	Early Sync Enabled				
TDM Channel Size 32-bit 👻	Rx Interleave Disabled				
	Tx Interleave Disabled				
Sync Mode 50 % Duty Cycle	Tx0 Enabled				
Sync Polarity Falling Edge	Tx1 Disabled				
DRXn Sampling BCLK Falling Edge	Rx0 Enabled				
DTXn Change BCLK Rising Edge	Rx1 Disabled				
Sync Offset	Clock Sustain Enabled				
- PDM					
PDM Rate SFF 👻	High Pass Filter Disabled				
PDM0 Slots 1-Slot - Rising Edge	PDM0 Disabled				
PDM1 Slots 1-Slot - Rising Edge	PDM1 Disabled				
PDM Data Out On Bus Only 💌	Alt. Clock on IO7 Inv. on BCLK				
Config and Control Slot Config Audio Config Rate and ClkOut Interrupt Config Pin Config ()					
Apply change to other nodes					
Master Address 0x68 Bu	s Address 0x69 😲				
A-Side Cable Length (m) 4.0	Use Configuration from EEPROM				

Figure 24 Audio Config tab settings example

If the connected device needs a MCLK that can be set in the dialog shown in the Figure 25. Clock out 2 (the module's A3 pin) is used to drive MCLK. This is a multipurpose pin, it's IO2 and ADR2 as well.

AD242x Slave Clkwrks EV	M Properties			
General View Register View	V Stream View		~	
I2S Rate Settings]	
I2S Rate	SFF x 1 👻	Reduce/Retransmit	Disabled	
Share Slots(RR)	Disabled			
Reduced Rate Controls				
Strobe Direction	Input -	Strobe in IO7	Disabled	
Reduce Rate Valid bit(s) in	LSB	Extra Bit	
Sync Offset	0 -			
Clock Out1		Clock Out2		
Enable Clock Out1		Enable Clock Out2	2	
Pre Div Factor 1	2 💌	Pre Div Factor 2	2 🗸	
Post Div Factor1	2 💌	Post Div Factor2	4 👻	
Clock1 Invert	Disabled	Clock2 Invert	Disabled	
Clock1 Output(Hz)	24576000	Clock2 Output(Hz)	12288000	
Config and Control Slot Config Audio Config Rate and ClkOut Interrupt Config Pin Config				
Apply change to other nodes				
Master Address 0x68 Bus Address 0x69				
A-Side Cable Length (m) 4.0)	Use Configuration	from EEPROM	

Figure 25 Rate and ClkOut tab settings for ADAU1761 default EVM program

5.3 ACCESSING THE LED AND SWITCH FROM SIGMA STUDIO

GPIO can be accessed from the AD2428 block in Sigma Studio by right clicking on the block associated with the EVM board. There are two ways to do this, one at a low level of direct register access, like what a program would do, and the other via the more convenient "General View," though that second method only helps for output, i.e. turning the LED on and off.

5.3.1 THE HARD WAY

Select Register View and the IO tab. For details of the registers and their bit maps please see the AD242x Programmers Reference Manual.

A2B Slave Nod	e1 WBZ Propertie	25					
General View Re	egister View Strea	m View	9				
Pin IO and Int	errupt Registers						
	Register	Register Address	Register Value				
	CLK1CFG	(0x59)	0x00				
	CLK2CFG	(0x5A)	0xC1				
	GPIODAT	(0x4A)	0x10				
	GPIODATSET	(0x4B)	0x10				
	GPIODATCLR	(0x4C)	0x10				
	GPIOOEN	(0x4D)	0x10				
	GPIOIEN	(0x4E)	0x41				
	GPIOIN	(0x4F)	0x40				
	PINTEN	(0x50)	0x00				
	PINTINV	(0x51)	0x00				
	PINCFG	(0x52)	0x00				
	Select All						
Config and Cont	Config and Control Slot Config I2C,I2S/PDM Interrupt and Error IO PRBS Status I						
Select All Re	Select All Register Groups						
		Nedu					
Master Address	0x68	Bus Address	s 0x69 😲				
A-Side Cable Length (m) 4.0 💼 🔲 Use Configuration from EEPROM							

Figure 26 IO tab in SigmaStudio

To operate the LED first write 0x01 to the GPIOOEN register (0x4D). Then place 0x01 in the GPIODATSET or GPIODATCLR register and write that to turn the LED on and off. The LED is connected on the AB0106 to the IO0 pin of the AD2428.

To read the switch write 0x80 to GPIOIEN register (0x4E). The switch is connected to IO7. Select GPIOIN and hit the Read button to see the switch value in the highest bit position. A zero in this bit position means the button is pushed.

5.3.2 THE EASY WAY

This will allow turning the EVM's LED on and off, which might be useful to confirm the node you've selected is the one you think it is. On the General View tab select the Pin Config dialog and set GPIO0 to be an output. High turns the LED on, Low shuts it off.

General View R	egister View Stream V	îew		9
General Pum	ose Input/Output			
GPIO0	OUTPUT -	Low		
GPIO1	DISABLE 👻			
GPIO2	CLKOUT 👻			
GPIO3	DTX0 -			
GPIO4	DISABLE 👻			
GPIO5	DRX0 -			
GPIO6	DISABLE 👻			
GPIO7	INPUT -	Interrupt Disable	Rising Edge	
Pin Config				
IRQ Edge	e	Rising Edge	Sustain PLL on	-
IRQ Tris	tate	Disable		
Digital Pi	n Drive Strength	Low		
Config and Con	trol Slot Config Audi	o Config Rate and Clk	Out Interrupt Config Pin Conf	ig 💽
Apply chang	to other nodes			r
Master Address	0x68	Bus Ad	ldress 0x69	Y.
A-Side Cable Ler	aath (m) 4.0 🚔	🔲 Use	e Configuration from EEPROM	

Figure 27 AB0106 User LED (GPIO 0) control

6 CONFIGURING A ROOT NODE SETUP WITH THE AB0108

The example will use the AB0108 (with AB0003L module) for the root node and the A²B EVM board as an example downstream node as shown in Figure 28. To keep the example simple no audio sources are used, connectivity can be validated by toggling the user LED on the EVM.

An external source is needed for the SYNC signal. It must match the IOVDD settings used, which is 3.3 V with the AB0108. Even though it is only a 48 kHz signal the edges should be clean, it is suggested that the source use series termination and wire lengths should be kept reasonable. The external SYNC (and BCLK if using I²S) are buffered on the AB0108 before driving the AD2428.



Figure 28 AB0108 example hardware setup

Start with the supplied SigmaStudio example (AB0108_EVM.dsproj) or create a new project and add the host, AD2428, and AB0108 blocks as shown. If creating from scratch make sure you use the AD242x Master node for the first one.



Figure 29 AB0108 root node mode with Clockworks EVM client node mode example

For the client node EVM with the AB0001 module please see the user manual for that board.¹³ The remainder of this section will just look at the root node setup.

The 4 bit GPIO block is the PCA9536 I²C expander. The block's properties are set to enable the SYNC as described in section 2.3.1.

¹³ https://clk.works/products/a2b-products/a2b-module-evm/

A2B Master Node Clockworks EVM Propertie	es 📃 🗖 X
General View Register View Stream View	
Master Config	Calculate Response Cycles
I2C Early Ack Disabled	Node Response Cycles
Data Out on Bus Monitor Disabled	M - 4 🐳 x N
	M - Master Node Reponse Cycles
	N - Slave Node Index
	☑ Update Slave Node Resp cycles
Up/Down Stream Settings	
Upstream Enable Disabled	Downstream Enable Enabled
Upstream Slot Size	Downstream Slot Size 24-bit 👻
Upstream Compression Disabled	Downstream Compression Disabled
Slot Rate	
Reduced Rate on Bus	Sys Rate Divide 1
Spread Spectrum Settings	
Mode No Spread -	Frequency 4x -
Depth () Low () High	
Config and Control Audio Config Rate and Clk	Out Interrupt Config Pin Config GPIOD ID
Apply change to other nodes	
Master Address 0x68 🗸	Bus Address 0x69
	0

Figure 30 Root node properties

This simple example does not use any $I^2S I/O$ on the root node. If your setup will include audio devices connected to the AB0108 you will need to set the I^2S register settings. For the AD2428 this can be set directly in its properties:

A2B Master Node Clockworks EVM Properties					
General View Register View Stream View		5			
125					
TDM Mode TDM8 -	Early Sync	Enabled			
TDM Channel Size 32-bit 🗸	Rx Interleave	Disabled			
	Tx Interleave	Disabled			
Sync Mode 50 % Duty Cycle	Tx0	Enabled			
Sync Polarity Falling Edge	Tx1	Disabled			
DRXn Sampling BCLK Rising Edge	Rx0	Enabled			
DTXn Change BCLK Falling Edge	Rx1	Disabled			
Tx Offset	Tri-state Before Tx	Disabled			
Rx Offset 0	Tri-state After Tx	Disabled			
PDM P-te	Lish Deep Filter	Displied			
		Disabled			
PDM0 Slots I-Slot V Rising Edge Y	PDMU	Disabled			
PDM1 Slots 1-Slot V Rising Edge	PDM1	Disabled			
PDM Data Out On Bus Only	Alt. Clock on IO7				
Config and Control Audio Confin Rate and ClkOut Interrupt Config Pin Config GPIOD ID					
Apply change to other nodes					
Master Address 0x68 - Bus	s Address Ox69				

Figure 31 Root node example settings for TDM8 over I²S

7 CONFIGURING A ROOT NODE SETUP WITH THE AB0110

The AB0110 includes a 12.228 MHz oscillator and dividers to create BLCK and SYNC signals. The BCLK signal must be selected to match the TDM mode being used for I²S data. If using the AB0110 as a root node without I²S data then the selection of BCLK is not important as it's only used by the AD2428 for data clocking. See Section 2.4 for the jumper settings.

Figure 32 shows the hardware setup used for this example. If it looks almost identical to Figure 28 that is because it is; the only real difference is an external 48 kHz SYNC signal is not needed since the AB0110 include clock generation.



Figure 32 AB0110 and EVM board example

The example schematic is also pretty much the same one as for the AB0108, the only important difference is the polarity of the IO1 bit is opposite for enabling the SYNC signal.



Figure 33 SIgmaStudio example for AB0110

If external I^2S devices (ADC and/or DACs) are needed on the root node they can be connected to the I^2S header. Since the AB0110 generates SYNC and BLCK hookup is generally pretty easy.

The same settings as illustrated in Section 6 for the AB0108 need to be review for the I²S connections you will use. Don't forget the BLCK jumper must match the intended TDM mode.









<i>Iaster I/O expander with clock output</i>				
abloid	Number: AB0110	Revision:2		
/14/2020	Time: 11:05:11 PM	Sheet 1 of 1		
B0110.M	cO.simpleIO.SchDoc			
-				